Over the years, the device density has increased together with some increase in the chip area. Figure 1.2 (a, b, c) show small (SSI), medium (MSI) and large (LSI or VLSI) IC chip size. The chip areas range from 1 mm^2 (1600 mil^2)* for the SSI chip to 1 cm^2 (1,60,000 mil^2) for the LSI chip.

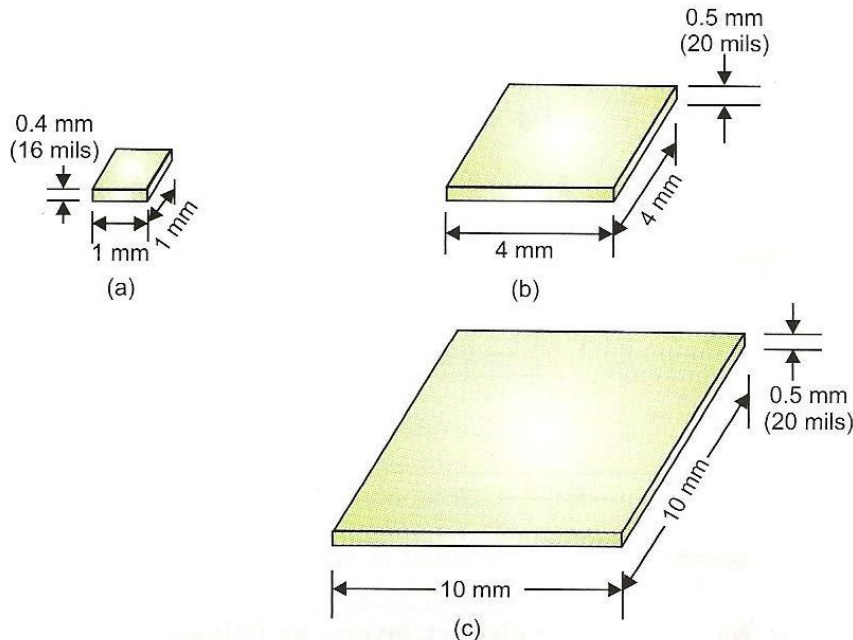

Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

1.4 FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

A monolithic circuit, literally speaking, means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek word *monos* meaning 'single' and *lithos* meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

The most significant advantage of integrated circuit of reducing the cost of production of electronic circuits due to batch production can be easily visualized by a simple example. A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously. Many chips so produced will be faulty due to imperfection in the manufacturing process. Even if the yield (percentage of fault free chips/wafer) is only 20 per cent, it can be seen that 16,000 good chips are produced in a single batch.

The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit of Fig. 1.3 when fabricated by silicon planar technology will have the cross-sectional view shown in Fig. 1.4.

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* mil = 0.001 in = 25.4 μm = 0.0254 mm

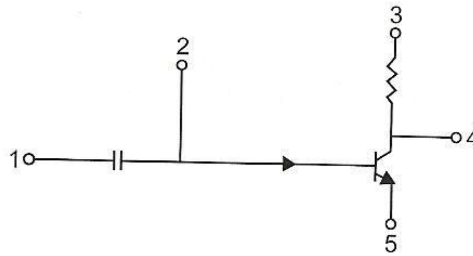


Fig. 1.3 A typical circuit

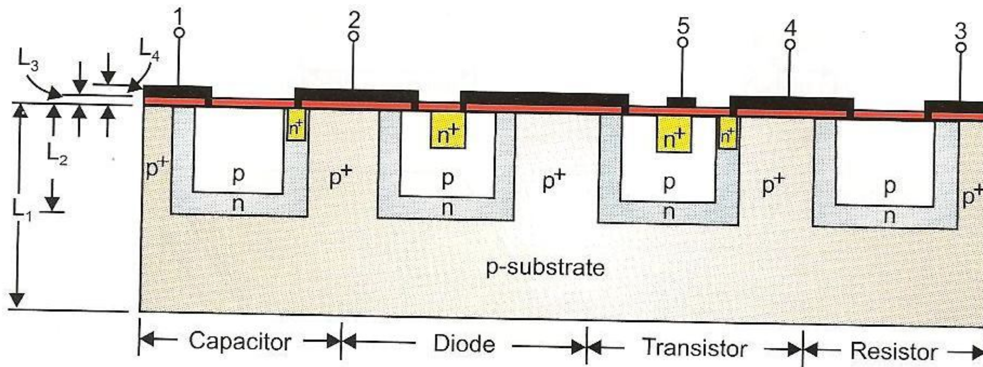


Fig. 1.4 Complete cross-sectional view of the circuit in Fig. 1.3 when transformed into monolithic form

An IC in general, consists of four distinct layers, as follows:

Layer No. 1 (~ 400 μm) is a *p*-type silicon substrate upon which the integrated circuit is fabricated.

Layer No. 2 (~ 5–25 μm) is a thin *n*-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.

Layer No. 3 (0.02–2μm) is a very thin SiO_2 layer for preventing diffusion of impurities wherever not required using photolithographic technique.

Layer No. 4 (~ 1μm) is an aluminium layer used for obtaining interconnection between components.

It may be pointed out that the drawings showing the cross-sectional view in this chapter are never scale drawings, but are distorted for the particular emphasis required.

1.5 BASIC PLANAR PROCESSES

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation techniques

8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail.

1.5.1 Silicon Wafer Preparation

The following steps are used in the preparation of Si-wafers:

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a *seed crystal* is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.

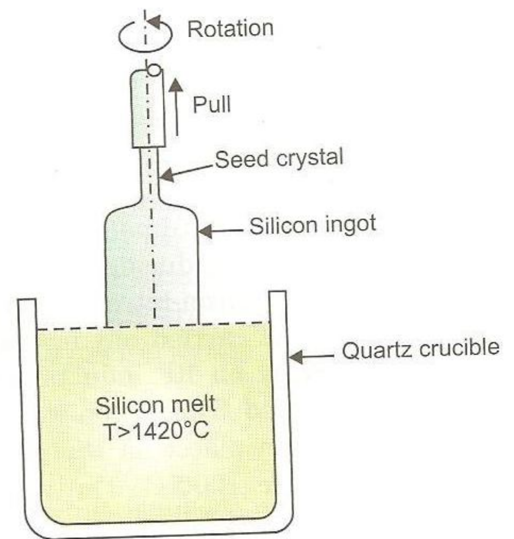


Fig. 1.5 Czochralski crystal growth

Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter (D = 10, 12.5, 15 cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then sliced using a stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in Fig. 1.6. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other

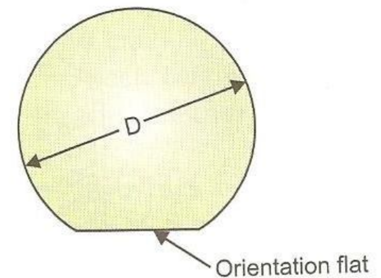


Fig. 1.6 Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

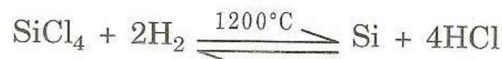
side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23–40 mils produces wafers of 16–32 mils thickness after all the polishing steps.

These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit. After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

1.5.2 Epitaxial Growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.



$$SiCl_4 + 2H_2 \xrightleftharpoons{1200^\circ C} Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the n-type and bi-borane (B_2H_6) for p-type doping into the silicon-tetrachloride hydrogen gas stream.

The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a *boat*. This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C. The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

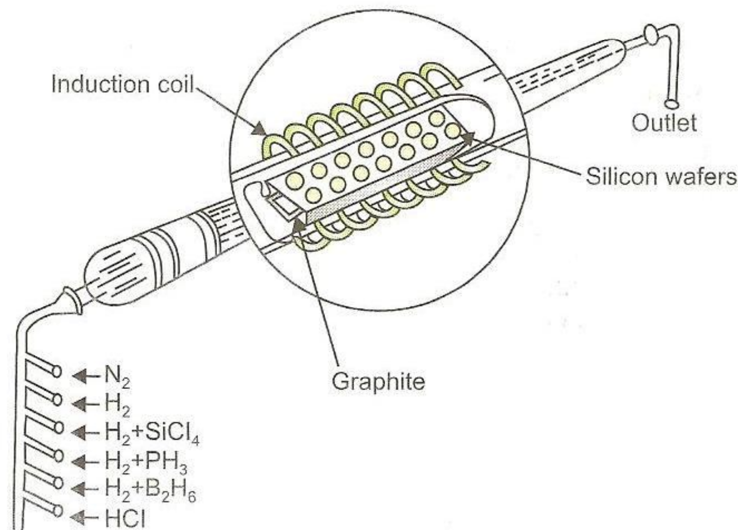


Fig. 1.7 A diagrammatic representation of a system for growing silicon epitaxial films

1.5.3 Oxidation

SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus, it stands against any contamination.
2. By selective etching SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing O_2 or H_2O or both. The chemical reaction is

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

This oxidation process is called *thermal oxidation* because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.

1.5.4 Photolithography

With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers. As many as 10,000 transistors can be fabricated on a 1 cm × 1 cm chip. The conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2 μm can be obtained. However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become possible to produce device dimension down to sub-micron range (<1 μm).

Photolithography involves two processes, namely:

Making of a photographic mask

Photo etching

The making of a photographic mask involves the following sequence of operations—first the preparation of initial artwork and secondly, its reduction. The initial layout or artwork of an IC is normally done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. This is because, for a tiny chip, larger the artwork, more accurate is the final mask. For example, it is often required to make an opening of width about 1 mil (25 μm). Obviously, this cannot be managed by any draftsman even with his thinnest of sketch pens. So the drawings are made magnified and often by a factor of 500. With this magnification, it is easy to see that a width of one mil is magnified to a width of 500 mils, that is, about 1.2 cm. Therefore, for a finished monolithic chip of area 50 mils × 50 mils, the artwork will be made on an area of about 60 cm × 60 cm.

This initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule, e.g., a mask for base diffusion, another for collector diffusion, another for metallization and so on.

For photographic purpose, artwork should not contain any line drawings but must be of alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque mylar (trade name-Rubylith). The red layer can be easily peeled off thus exposing clear areas with a knife edge from the regions where impurities have to be diffused. The artwork is usually produced on a precision drafting machine, known as *coordinatograph*. The coordinatograph has a cutting head that can be

positioned accurately and moved along two perpendicular axes. The coordinatograph outlines the pattern cutting through the red mylar without damaging the clear layer underneath.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image also must be repeated many times in a matrix array, so that many ICs will be produced in one process. The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposure, the plate is moved in equal steps so that successive images form in an array. When the exposed plate is developed, it becomes a master mask. The masks, actually used in IC processing are made by contact printing from the master. These working masks wear out with use and are replaced as required.

Photo-etching is used for the removal of SiO_2 from desired regions so that the desired impurities can be diffused. The wafer is coated with a film of photosensitive emulsion (Kodak Photoresist KPR). The thickness of the film is in the range of 5000–10000 Å as shown in Fig. 1.8 (a). The mask negative of the desired pattern) as prepared by steps described earlier is placed over the photoresist coated wafer as shown in Fig. 1.8 (b). This is now exposed to ultraviolet light, so that KPR becomes polymerized beneath the transparent regions of the mask. The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed/unpolymerized regions on the photoresist and leaves the pattern as shown in Fig. 1.8 (c). The polymerized photoresist is next fixed or cured, so that it becomes immune to certain chemicals called *etchants* used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the SiO_2 from the areas which are not protected by KPR as shown in Fig. 1.8 (d). After diffusion of impurities, the photoresist is removed with a chemical solvent (hot H_2SO_4) and mechanical abrasion.

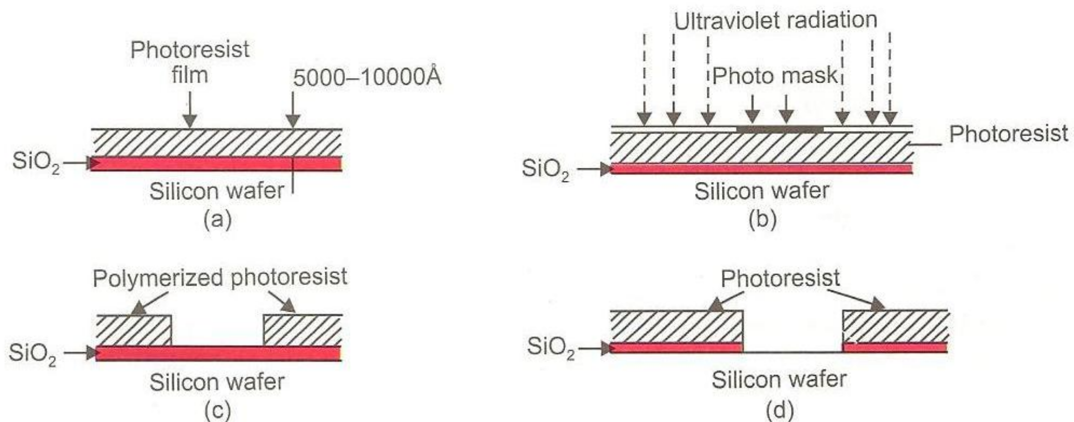


Fig. 1.8 Various steps for photo-etching

The etching process described is a wet etching process and the chemical reagents used are in liquid form. A new process used these days is a dry etching process called *plasma etching*. A major advantage of the dry etching process is that it is possible to achieve smaller line openings (≤1 μm) compared to wet process. Complete description of the plasma etching process is beyond the scope of this book.

X-Ray and Electron Beam Lithography

With conventional ultraviolet (UV) photolithography process in which the UV wavelengths used are in the range, 0.3 to 0.4 μm, the minimum device dimensions or line widths are

limited by diffraction effects to around five wavelengths or about 2 μm. This is what puts an upper limit on the IC device density using UV photolithography.

With the advent of X-ray and electron beam lithography techniques, it has become possible to produce device dimensions down to submicron range (<1 μm). This is due to much shorter wavelengths involved. With these techniques, MOSFET with gate length as small as 0.25 μm have been made. The cost of X-ray or electron beam equipment is very high and the exposure time is very much longer than UV photolithography. So this becomes a very expensive process and is used only when very small device dimensions (≤1 μm) are needed.

1.5.5 Diffusion

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20″ length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C. Impurities to be diffused are rarely used in their elemental forms. Normally, compounds such as B_2O_3 (Boron oxide), BCl_3 (Boron chloride) are used for Boron and P_2O_5 (Phosphorous pentaoxide) and $POCl_3$ (Phosphorous oxychloride) are used as sources of Phosphorous. A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.

The diffusion of impurities normally takes place both laterally as well as vertically. Therefore, the actual junction profiles will be curved as shown in Fig. 1.9. However, for the sake of simplicity, lateral diffusion will be omitted in all the drawings.

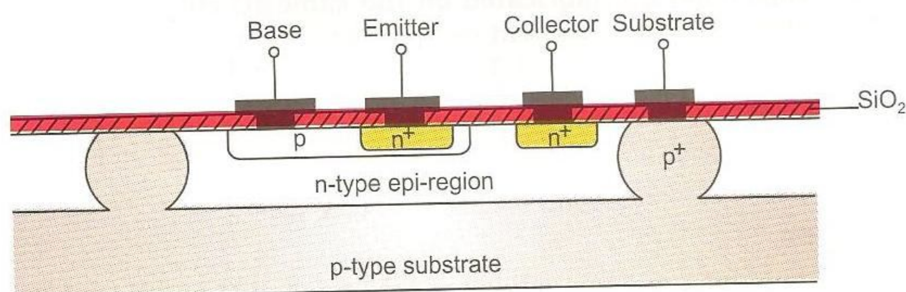


Fig. 1.9 The cross-section of an *npn* transistor showing curved junction profiles as a result of lateral diffusion

1.5.6 Ion Implantation

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high-energy dopant ions (borons for p-type and phosphorus for n-type) as shown in Fig. 1.10. These ions are accelerated by energies between 20 kV to 250 kV. As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage. Ion implantation technique has two important advantages.

1. It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.

2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.

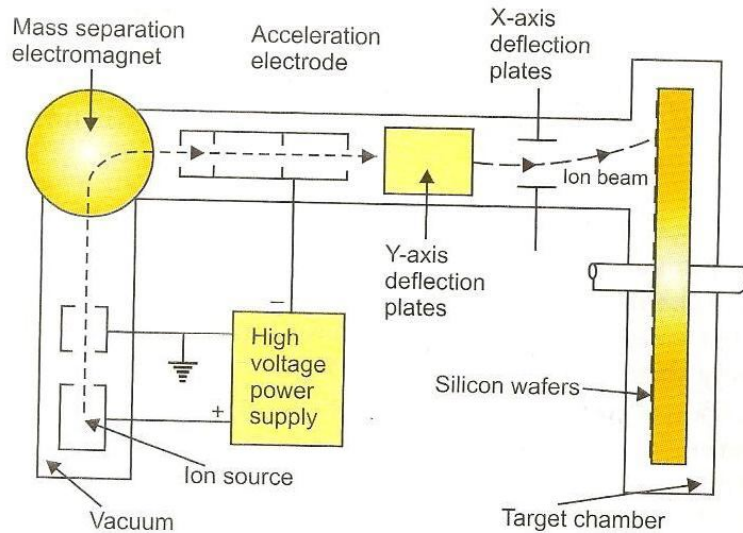


Fig. 1.10 Ion implantation system

1.5.7 Isolation Techniques

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques, namely:

p-n junction isolation
Dielectric isolation

p-n Junction Isolation

In this isolation technique, p^+ type impurities are selectively diffused into the n-type epitaxial layer so as to reach p-type substrate as shown in Fig. 1.11 (a). This produces islands surrounded by p-type moats. It can be seen that these regions are separated by two back-to-back p-n junction diodes. If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse biased providing electric isolation between these islands. The different components are fabricated in these isolation islands. The concentration of the

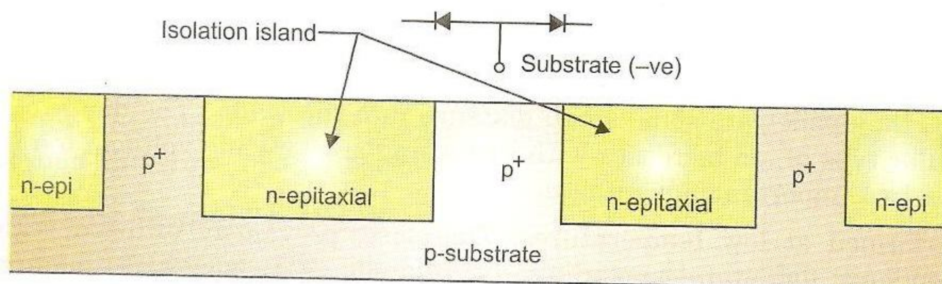


Fig. 1.11 (a) *p-n* junction isolation

acceptor atoms in the region between isolation islands is usually kept much higher (p^+) than the p-type substrate. This prevents the depletion region of the reverse biased diode from penetrating more into p^+ region and possibly connecting the isolation islands.

There is, however, one undesirable by-product of this isolation process. It is the presence of a transition capacitance at the isolating pn junctions, resulting in an inevitable capacitor coupling between the components and the substrate. These parasitic capacitances limit the performance of the circuit at high frequencies. But being economical, this technique is commonly used for general purpose ICs.

Dielectric Isolation

Here a layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical. This isolating dielectric layer is thick enough so that its associated capacitance is negligible. Also, it is possible to fabricate both *pnp* and *npn* transistor within the same silicon substrate. Since this method requires additional fabrication steps, it becomes more expensive. The technique is mostly used for fabricating professional grade ICs required for specialised applications viz, aerospace and military, where higher cost is justified by superior performance. Figure 1.11 (b) shows such a structure.

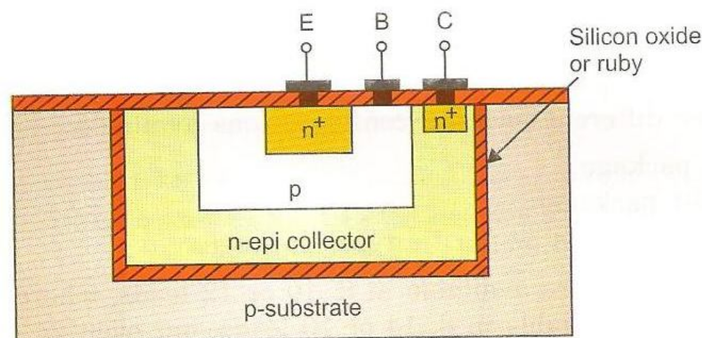


Fig. 1.11 (b) Dielectric isolation

1.5.8 Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages.

1. It is relatively a good conductor.
2. It is easy to deposit aluminium films using vacuum deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, non-rectifying (i.e., ohmic) contact with p-type silicon and the heavily doped n-type silicon.

The film thickness of about 1 μm and conduction width of about 2 to 25 μm are commonly used. The process takes place in a vacuum evaporation chamber as shown in Fig. 1.12. The pressure in the chamber is reduced to the range of about 10^{-6} to 10^{-7} torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focussed at the surface of the material to be evaporated. This heats up the material to very high temperature and

it starts vaporising. These vapours travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration. This is done by photolithographic process and aluminium is etched away from unwanted places by using etchants like phosphoric acid (H_3PO_4).

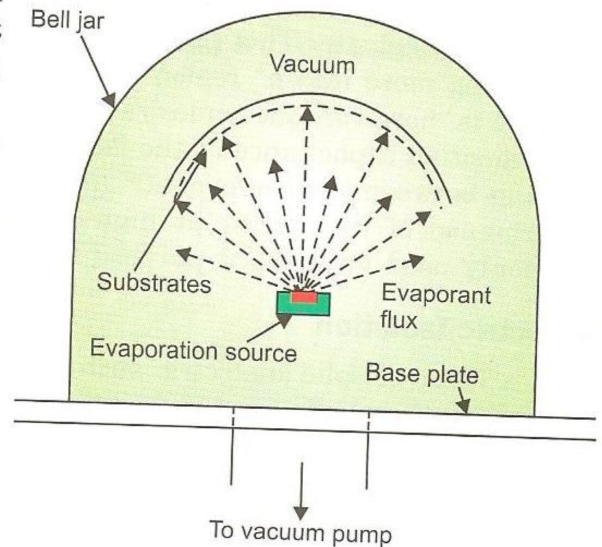


Fig. 1.12 Vacuum evaporation for metallization

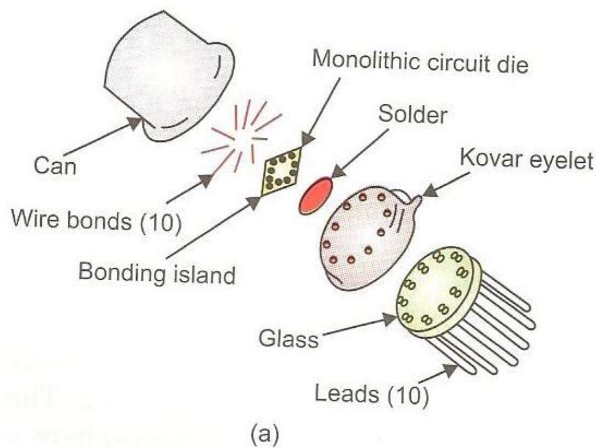
1.5.9 Assembly Processing and Packaging

Each of the wafer processed contains several hundred chips, each being a complete circuit. So, these chips must be separated and individually packaged. A common method called *scribing and cleaving* used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package.

There are three different package configurations available:

1. Metal can package
2. Ceramic flat package
3. Dual-in-line (ceramic or plastic type) package.

The metal can packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but even 24 or 36 or 42 leads are also available for special circuits. Ceramic packages, whether of flat type or dual-in-line are costly due to fabrication process, but have the advantage of best hermetic sealing. Most of the general



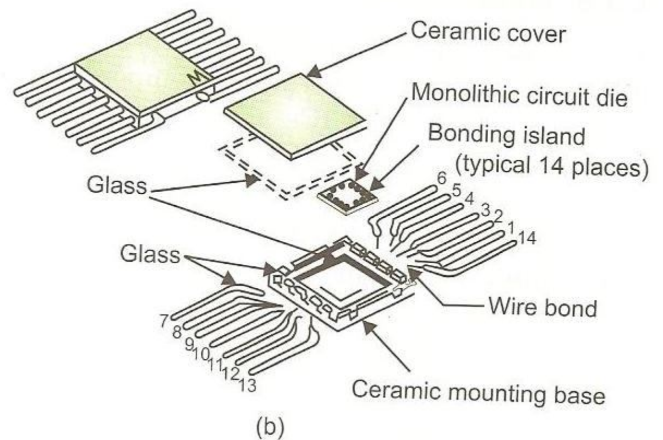


Fig. 1.13 Exploded view of (a) TO-5 metal can package (b) 14-lead version of the flat package, showing the various components as well as the completed flat package

purpose ICs are dual-in-line plastic packages due to economy. Figures 1.13 (a) and (b) shows the exploded view of TO-5 metal can and flat package respectively.

1.6 FABRICATION OF A TYPICAL CIRCUIT

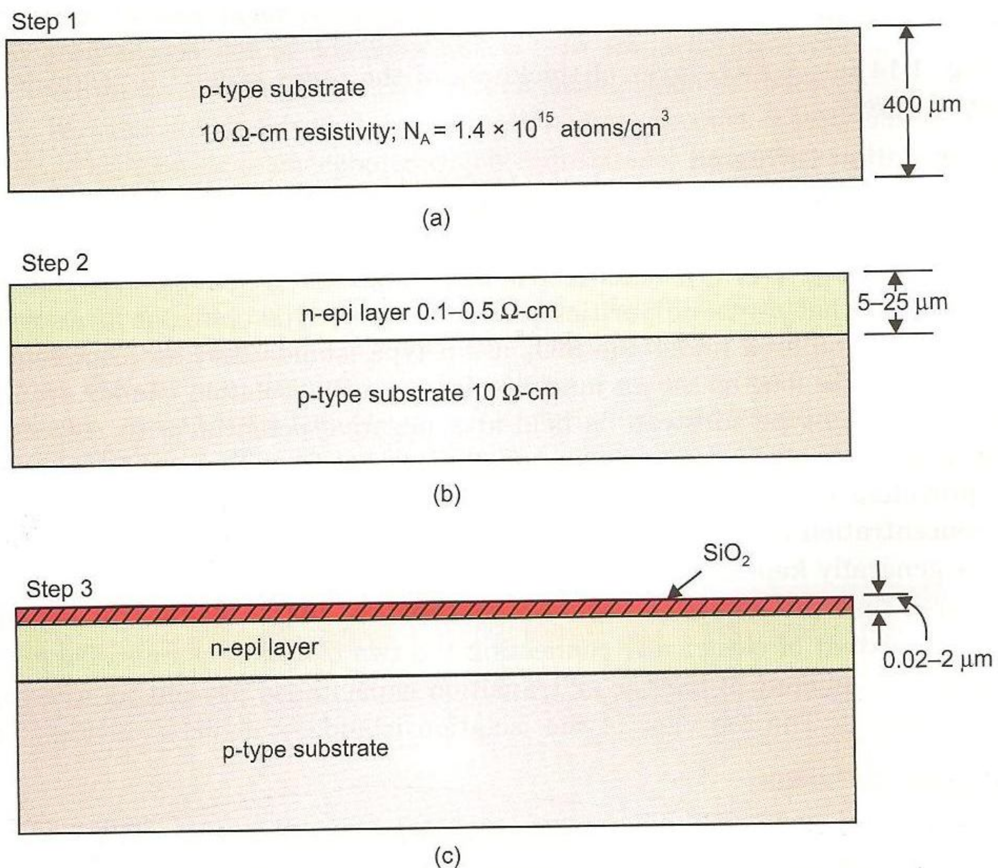
We shall here show the various steps utilized in converting the circuit of Fig. 1.3 into the monolithic IC of Fig. 1.4.

Step-1: Wafer Preparation

Refer Fig. 1.14 (a). The starting material called the substrate is a *p*-type silicon wafer prepared as discussed in Sec. 1.5.1. The wafers are usually of 10-cm diameter and 0.4 mm (~ 400 μm) thickness. The resistivity is approximately 10 Ω-cm corresponding to concentration of acceptor atom, $N_A = 1.4 \times 10^{15}$ atoms/cm^3.

Step-2: Epitaxial Growth

An *n*-type epitaxial film (5–25 μm) is grown on the *p*-type substrate as shown in Fig. 1.14 (b). This ultimately becomes the collector region of the transistor, or an element of the diode and diffused capacitor associated with the circuit. So, in general it can be said that all active and passive components are fabricated within this layer. The resistivity of *n*-epitaxial layer is of the order of 0.1 to 0.5 Ω-cm.



(Fig. 1.14 Contd.)

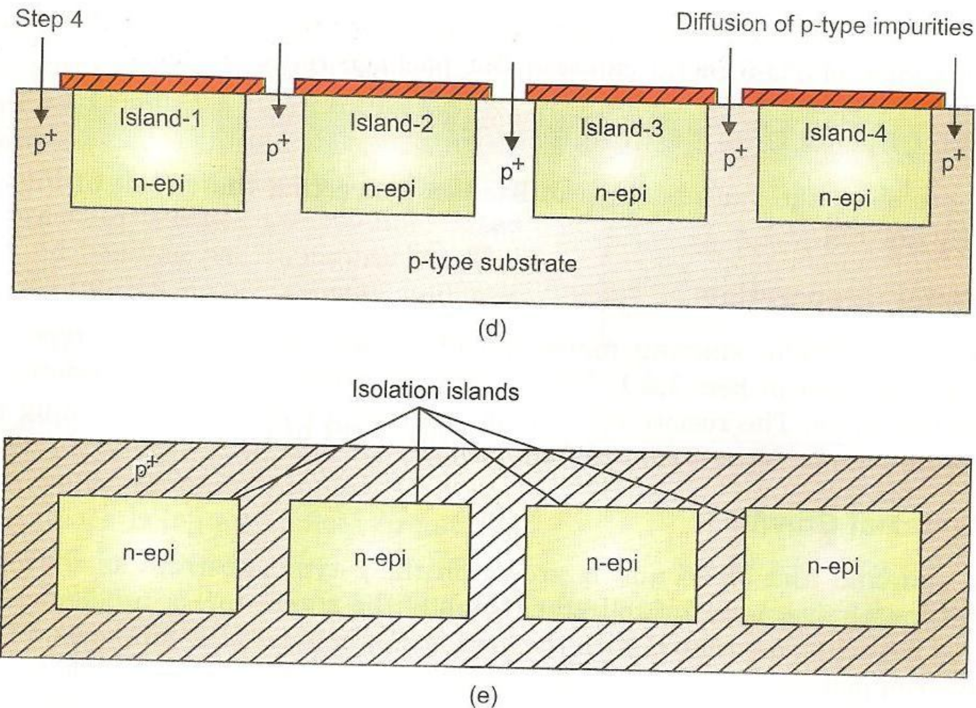


Fig. 1.14 (a–e) Steps in the fabrication of the circuit shown in Fig. 1.3

Step 3: Oxidation

Refer Fig. 1.14 (c). A SiO_2 layer of thickness of the order of 0.02 to 2 μm is grown on the n-epitaxial layer.

Step 4: Isolation Diffusion

In the circuit of Fig. 1.3, four components have to be fabricated, so we require four islands which are isolated. For this, SiO_2 is removed from five different places using photolithographic technique. Refer Fig. 1.14 (d). The wafer is next subjected to heavy p-type diffusion for a long time interval so that p-type impurities penetrate the n-type epitaxial layer and reach the p-type substrate. The area under the SiO_2 are n-type islands that are completely surrounded by p-type moats. As long as the pn junctions between the isolation islands are held at reverse bias, that is, the p-type substrate is held at a negative potential with respect to the n-type isolation islands, these regions are electrically isolated from each other by two back-to-back diodes, providing the desired isolation.

The concentration of acceptor atoms ($N_A \simeq 5 \times 10^{20}$ cm^{-3}) in the region between isolation islands is generally kept higher than p-type substrate for which $N_A = 1.4 \times 10^{15}$ atoms/cm^3. This ensures that the depletion region of the reverse biased diode will not extend into p^+ region to the extent of electrically connecting the two isolation islands. There will, however, be a significant amount of barrier or transition capacitance present as a by product of the isolation diffusion. The top view of the isolation islands is depicted in Fig. 1.14 (e).

Step 5: Base Diffusion

Refer to Fig. 1.14 (f). A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique. Now, p-type impurities, such as

boron, are diffused through the openings into the islands of n-type epitaxial silicon. The depth of this diffusion must be controlled so that it does not penetrate through n-layer into the substrate. This diffusion is utilized to form base region, of the transistor, resistor, the anode of the diode and junction capacitor.

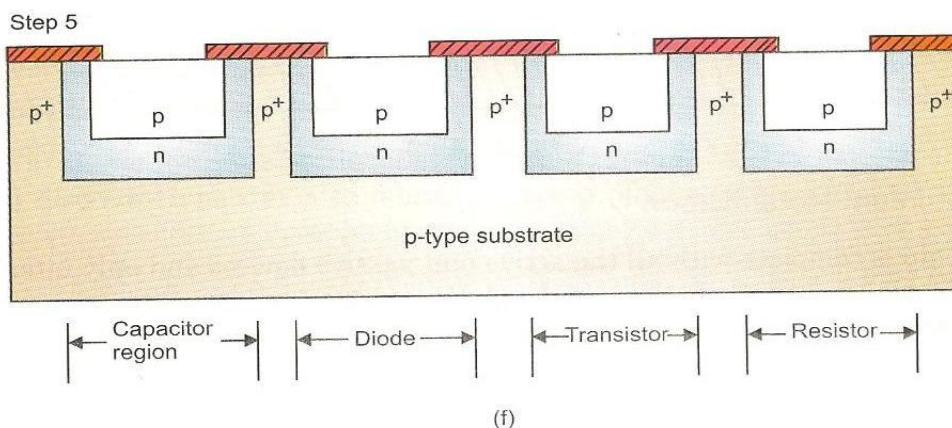


Fig. 1.14 (f)

Step 6: Emitter Diffusion

Refer to Fig. 1.14 (g). A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows and n-type impurity (phosphorus) is diffused through them. This forms transistor emitter and cathode region of diode.

Windows (W_1, W_2 etc.) are also etched into n-region where contact is to be made to the n-type layer. Heavy concentration of phosphorus (n^+) is diffused into these regions simultaneously with the emitter diffusion. The reason for using heavily-doped n-regions can be explained as follows:

Aluminium, normally used for making interconnections, is a p-type impurity in silicon, and can produce an unwanted rectifying contact with the lightly-doped n-material. However, heavy concentration of phosphorous ($\sim 2 \times 10^{20}$ cm^{-3}) doping causes a high degree of damage to the Si-lattice at the surface, thus effectively making it semi-metallic. This n^+ layer thus makes a good ohmic contact with the Al-layer. The top view corresponding to Fig. 1.14 (g) is shown in Fig. 1.14 (h).

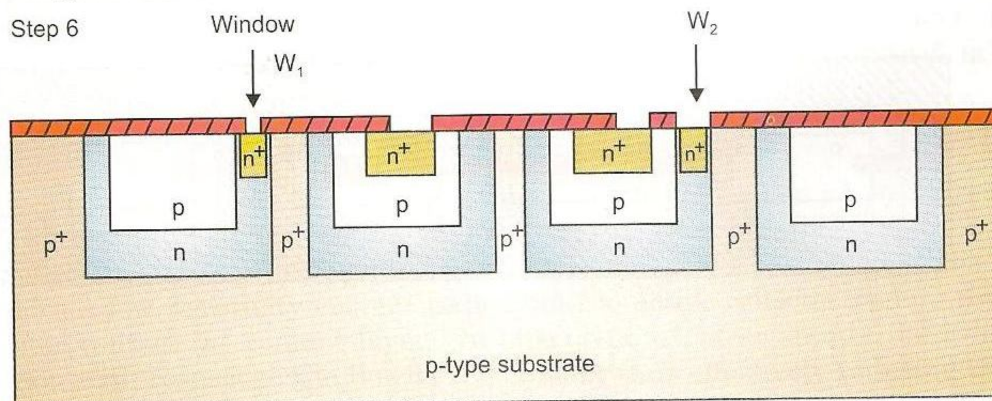


Fig. 1.14 (g)

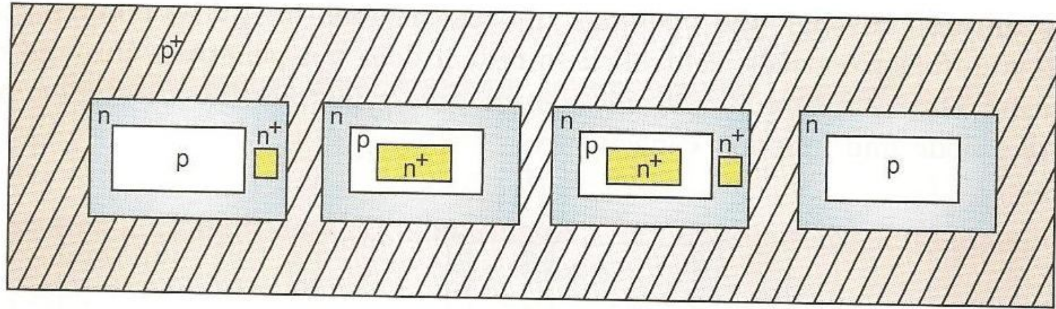
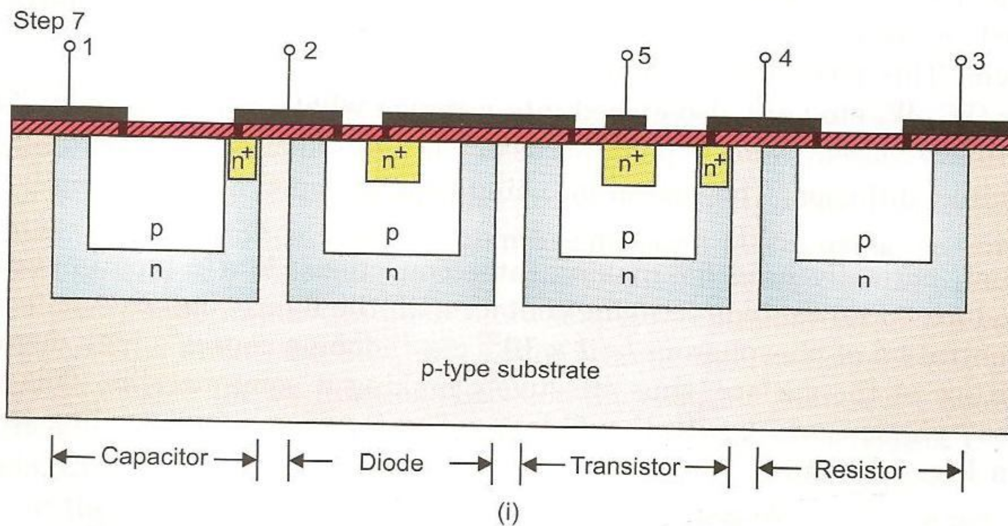


Fig. 1.14 (h)

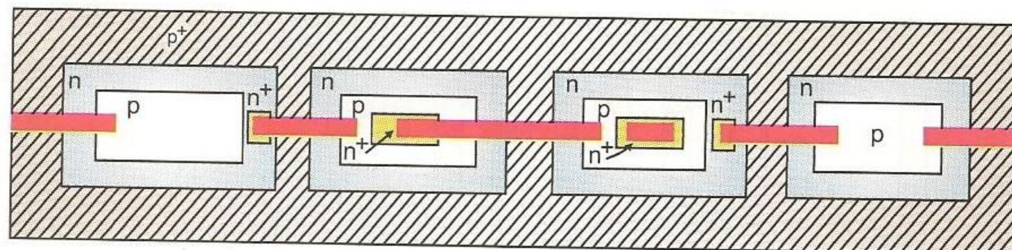
Step 7: Aluminium Metallization

Now the IC chip is complete with all the active and passive devices and only interconnections between the various components have to be made in accordance with the circuit in Fig. 1.3. The chip is further subjected to the process of the formation of a new SiO_2 layer and masked etching to open a new set of windows at the points where contacts have to be made.

Now, a thin even coating of aluminium is vacuum-deposited over the entire surface of the wafer. The interconnection pattern between the components is then formed by photo-resist techniques. The undesired aluminium areas are etched away leaving a pattern of interconnections between transistor, resistor, diode and capacitor as shown by the cross-sectional and top view in Fig. 1.14 (i) and Fig. 1.14 (j), respectively.



(i)



(j)

Fig. 1.14 (i, j)

parasitics, it requires a number of additional masking and deposition steps beyond the basic MOS structure. In such a structure, either aluminium or tantalum is used as capacitor plates and aluminium oxide (Al_2O_3) or tantalum oxide (Ta_2O_5) as the dielectric material. Ta_2O_5 is particularly preferred for large value capacitors. One basic serious disadvantage of thin film capacitor is that it fails when the voltage rating exceeds due to breakdown of the dielectric. This is a destructive and irreversible failure mechanism and may require over-voltage protection.

1.7.5 Integrated Inductors

Inductors, transformers and chokes are the missing link in the chain of IC components. IC devices are essentially two dimensional as the depth dimension is usually very small (~1 to 10 μm) compared to the lateral dimensions. IC inductors can be made in the form of a flat metallic thin film spirals by successive deposition of conduction patterns. Very small values of inductance of the order of nano-henry with low quality factor can be only obtained. For any reasonable inductance value, a three-dimensional coil structure is needed to obtain a large number of turns.

Most circuit designers go to great lengths to avoid the use of inductors or otherwise simulate them by using RC active networks. In applications such as RF and IF circuits, where inductors cannot be avoided, inductors external to the IC-package are used. However, in thin-film hybrid microwave integrated circuit (MIC), thin-film inductor spirals are used giving upto 250 nH.

1.8 FABRICATION OF FET

Unipolar monolithic ICs use JFET or MOSFET as an active device. The fabrication technique of JFET, MOSFET and CMOS is discussed.

1.8.1 JFET Fabrication

The structure of an n-channel JFET is shown in Fig. 1.26. The basic processes used are the same as in BJT fabrication. The epitaxial layer which formed the collector of the BJT is used as the n-channel of the JFET. The p^+ gate is formed in the n-channel by the process of diffusion or ion-implantation. The n^+ regions have been formed under the drain and source contact regions to provide good ohmic contact.

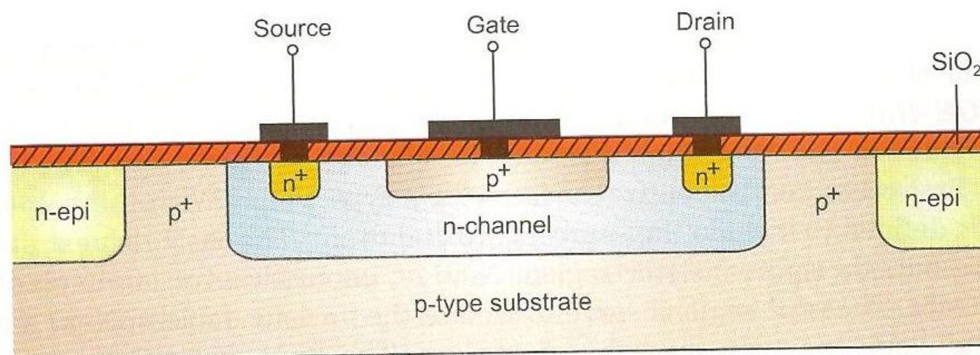


Fig. 1.26 n-channel JFET structure

1.8.2 MOSFET Fabrication

Two types of MOSFET devices are available, such as, enhancement type and depletion type. The cross-sectional view of n-channel aluminium gate enhancement MOSFET is shown in Fig. 1.27. In this structure, the metallic gate G is separated from the semiconductor channel by the insulating SiO_2 layer. The insulating layer of silicon dioxide gives an extremely high input resistance (10^{10} to 10^{15} Ω) for the MOSFET.

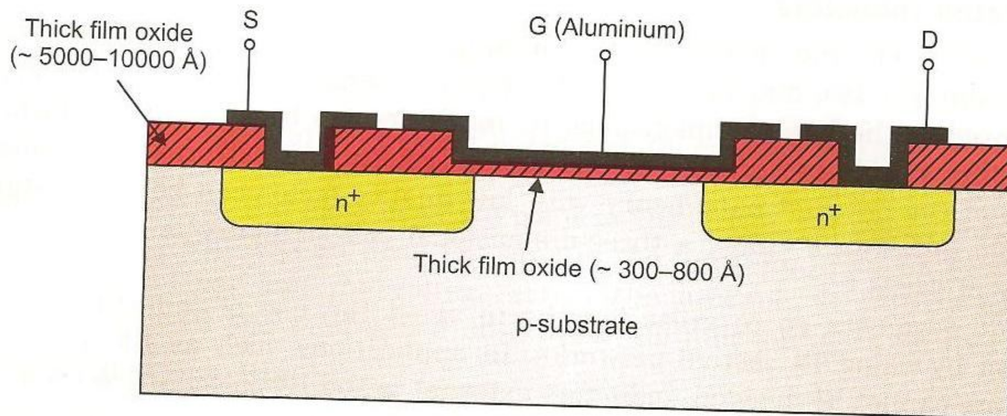


Fig. 1.27 *n*-channel MOSFET

The value of V_T, the threshold voltage for MOSFET fabricated by this technique is typically 3 to 6 V and power supply voltage of 12V is used for the drain supply. This large voltage is not compatible with the 5V supply used in digital ICs. A number of techniques have been developed to lower the magnitude of V_T which leads to improved device performance.

Use of Silicon Nitride (Si_3N_4)

It has been found that Si_3N_4 has superior masking properties compared to SiO_2. The Si_3N_4 is sandwiched between two SiO_2 layers and provides the necessary barrier to prevent impurities penetrating through the SiO_2 layer. The dielectric constant of Si_3N_4 is 7.5 whereas that of SiO_2 is 4. This increased overall dielectric constant reduces V_T.

Polysilicon Gate

Polycrystalline silicon when doped with phosphorus is conductive and is used as the gate electrode instead of aluminium. This reduces V_T to about 1 to 2 V. Such devices are called *silicon gate MOS transistors*. The fabrication of NMOS enhancement device using these improved techniques is shown in Fig. 1.28.

The Si_3N_4 is first coated on the entire surface of a p-type wafer. With the help of a mask, sufficient area is defined to include the source, gate and drain. The Si_3N_4 is next etched away from the surface outside the transistor region. Now p^+ impurities are ion-implanted in the exposed p-substrate. These p^+ regions serve to isolate the various devices. Next a thick SiO_2 layer called *field oxide* is grown over the p^+ regions. The Si_3N_4 region, however, remains unaffected by the oxidation. The structure now is as shown in Fig. 1.28 (a).

The Si_3N_4 is now removed by selective etching and then SiO_2 layer (800 to 1000 Å) is thermally grown over the transistor area as shown in Fig. 1.28 (b).