無線通訊系統
之積體電路設計(I)

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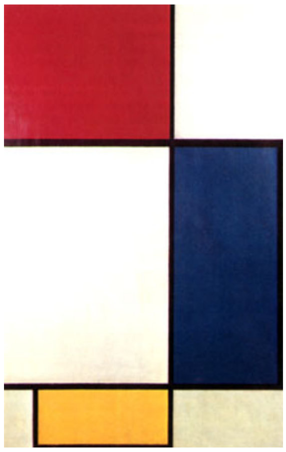
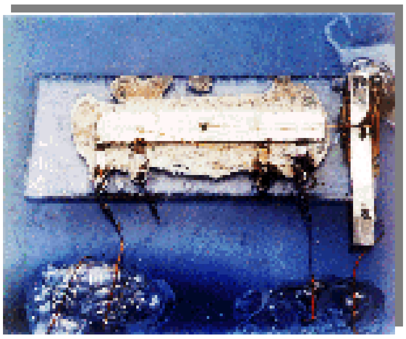


Outline

- Introduction of Wireless Communication System
- Analog Filter Design
- Switched Capacitor Filter Design
- Digital to Analog Circuit Design
- S/H Circuit Design
- Analog to Digital Circuit Design
- Appendix

Introduction of Chip Design

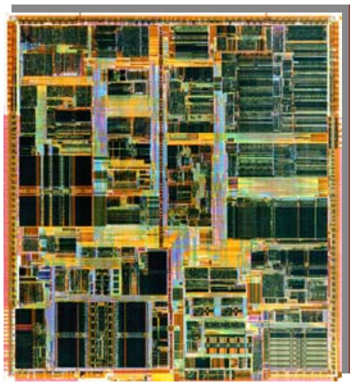
1958



First integrated circuit (germanium), 1958
Jack S. Kilby, Texas Instruments

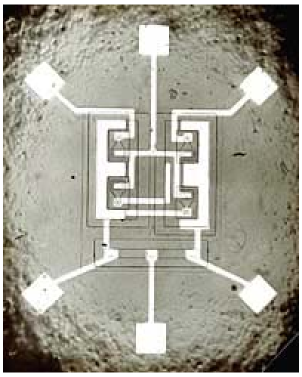
Contained five components, three types:
transistors resistors and capacitors

1997

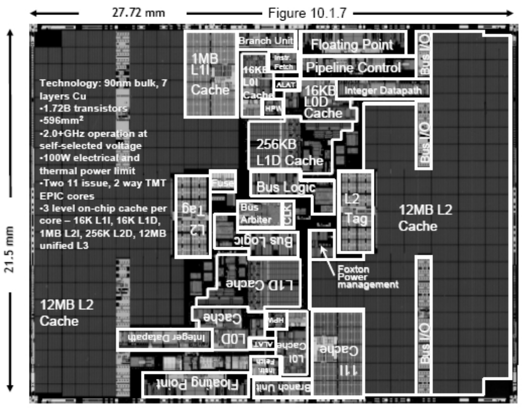


Intel Pentium II, 1997
Clock: 233MHz
Number of transistors: 7.5 M
Gate Length: 0.35 um

Chip Design: from 1961 to 2005

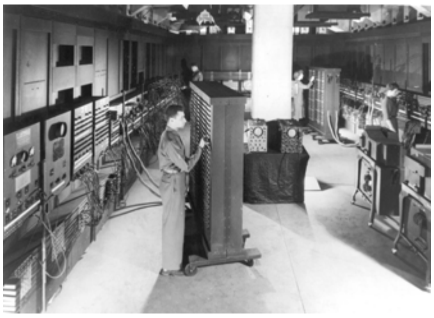


The first planar integrated circuit, 1960. Designed and built by Lionel Kattner and Isy Haas under the direction of Jay Last at Fairchild Semiconductor.



The Intel “Montecito” microprocessor, 2005.

Systems: from 1946 to 2005



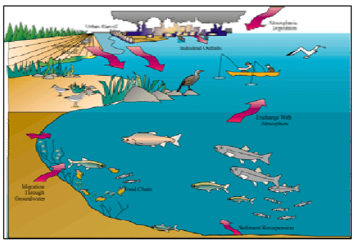
Original ENIAC machine at University of Pennsylvania
Speed: 5,000 additions or 10 multiplications/sec
* 17,500 vacuum tubes
* 174 KW
* 18,000 sq ft

INTEL P4, 90 nm CMOS
In this technology, it has:
-Area: 30x30 μm
-Power @ 1 MHz: 1 μW
-Potential speed: ~10 GHz

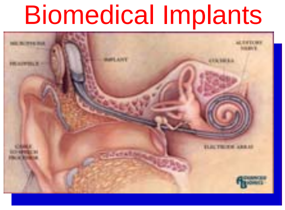
Wireless Integrated Microsystems (WIMS)

Environmental Sensors

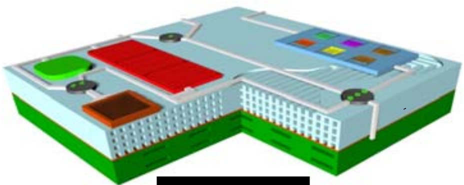
Heavy Metals



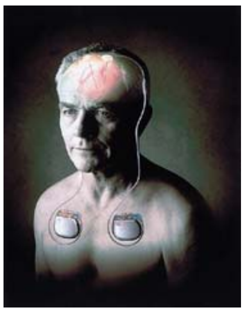
Biomedical Implants



Cochlear Implant



μ Gas Chromatograph



Deep Brain Implants

2002 and Beyond

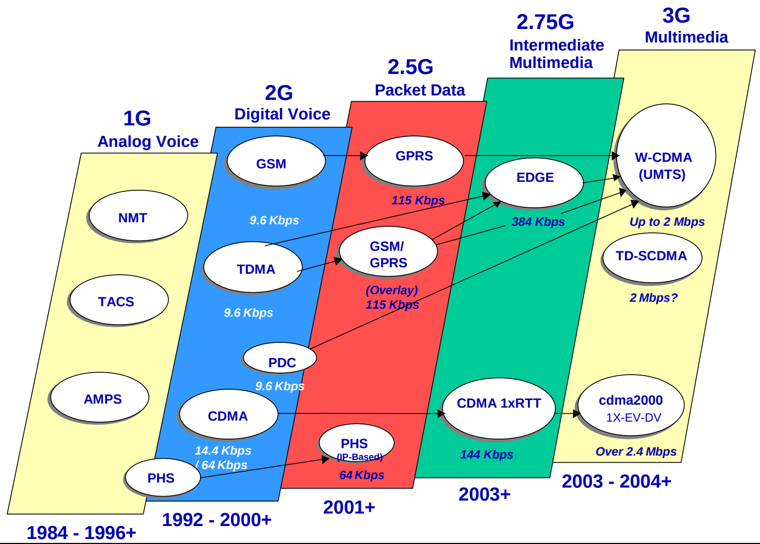
Semiconductor Industry Association (SIA) Road Map, 1998 Update

IEEE Spectrum, July 2009
Special report: "The 100-million transistor IC"

	1999	2002	2014
Technology (nm)	180	130	35
Minimum mask count	22/24	24	29/30
Wafer diameter (mm)	300	300	450
Memory-samples (bits)	1G	4G	1T
Transistors/cm² (μP)	6.2M	18M	390M
Wiring levels (maximum)	*6-7*	*7*	*10*
Clock, local (MHz)	1,250	2,100	10,000
Chip size: DRAM (mm²)	400	560	2240
Chip size: mP *(mm²)*	340	430	901
Power supply (V)	1.5-1.8	1.2-1.5	0.37-0.42
Maximum Power (W)	*90*	*130*	*183*
Number of pins (μP)	700	957	3,350

These scaling trends will allow the electronics market to growth at 15% / year.

The Evolution of Cellular Phone



Wireless Communication Standard

1-9

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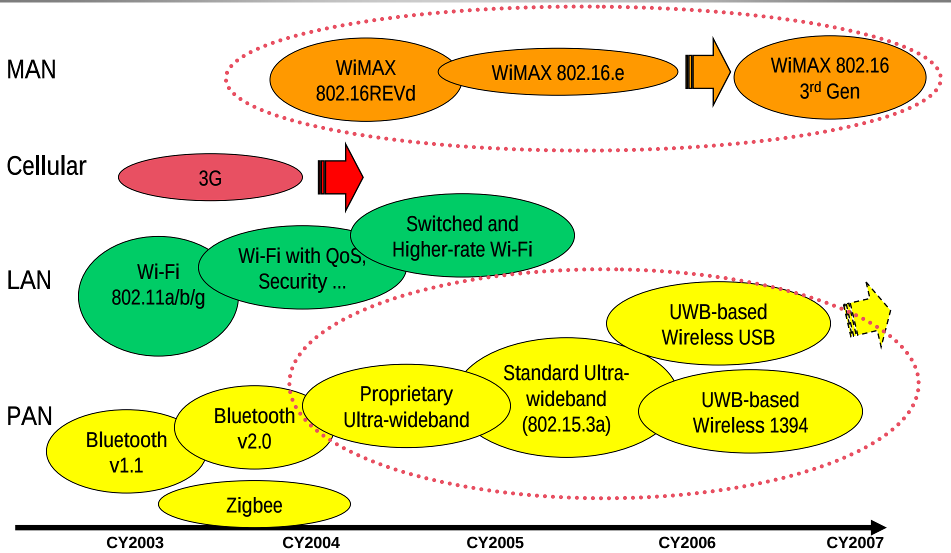

Wireless and Wire line Communication System

1-10

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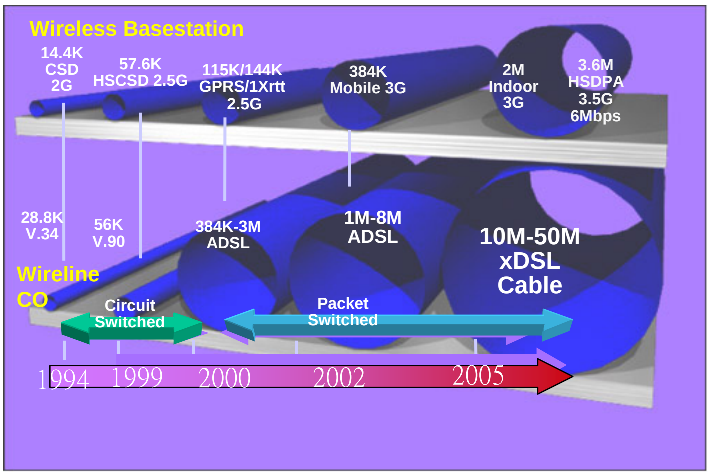
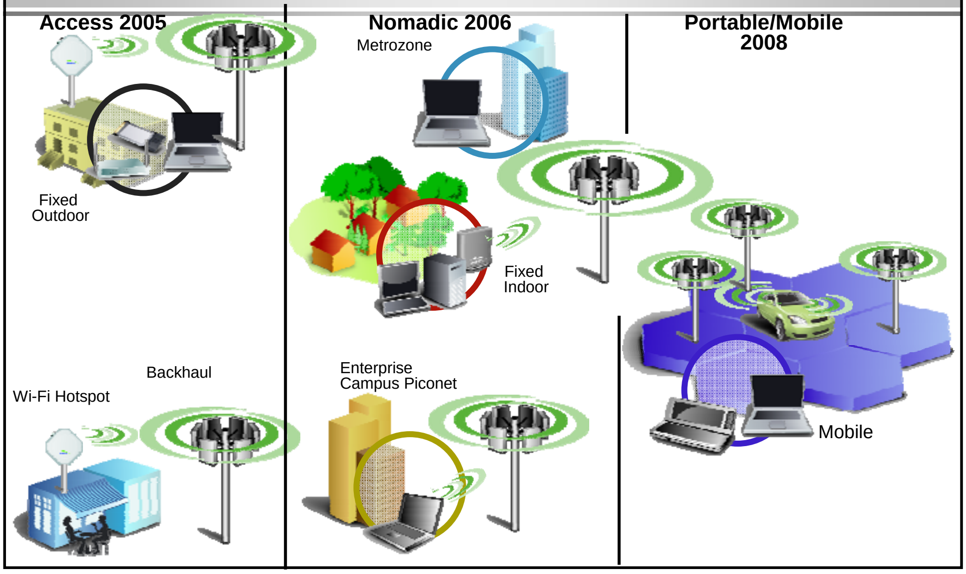
HSDPA: High-Speed Downlink Packet Access

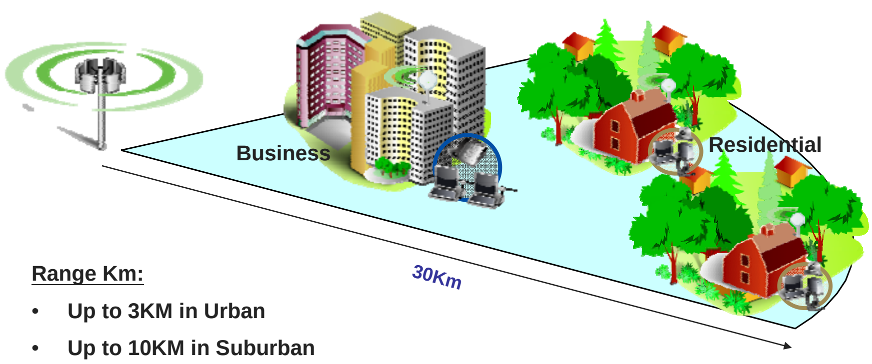


WiMAX Network Models



Fixed Wireless Broadband

Proprietary solutions moving to WiMAX standard :



Range Km:

- **Up to 3KM in Urban**
- **Up to 10KM in Suburban**
- **Up to 30KM in Rural**

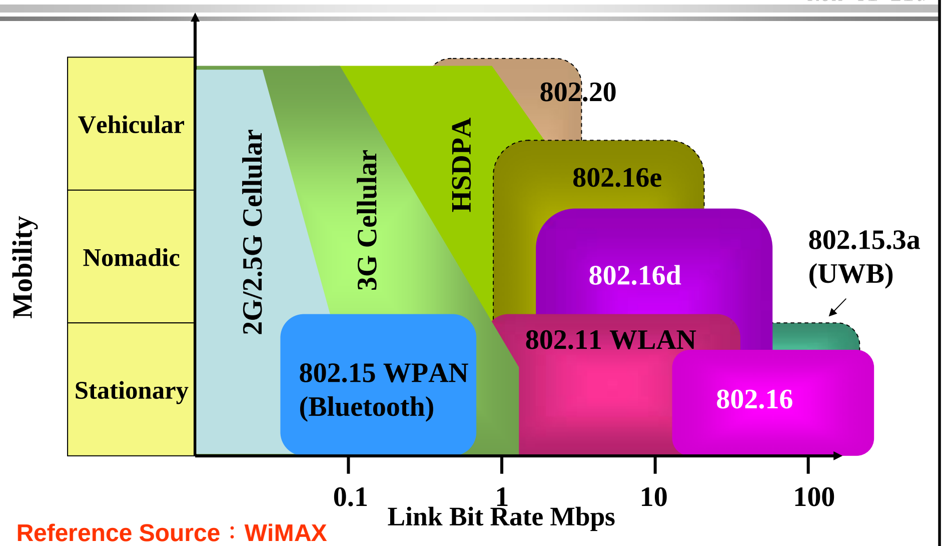
802.16 Communication Specification

標準	802.16	802.16-2004	802.16-2005
Bit Rate(Mbps)	32-134 (in 28MHz channel bandwidth)	Up to 75 (in 20MHz channel bandwidth)	Up to 15 (in 5MHz channel bandwidth)
Mobility	Fixed	Fixed,Portable	Fixed,Portable,Mobility
Spectrum(GHz)	10-66	<11	<6
Channel Conditions	Line of Sight only	Non Line of Sight	Non Line of Sight
Channel Bandwidths(MHz)	20,25,28	Scalable 1.5-20	Scalable 1.5-20
Typical Cell Radius (KM)	2-5	7-10 (Max Range 50)	2-5
Completed	2001/12	2004/06	2005/12

The Comparison of WiMAX and HSDPA

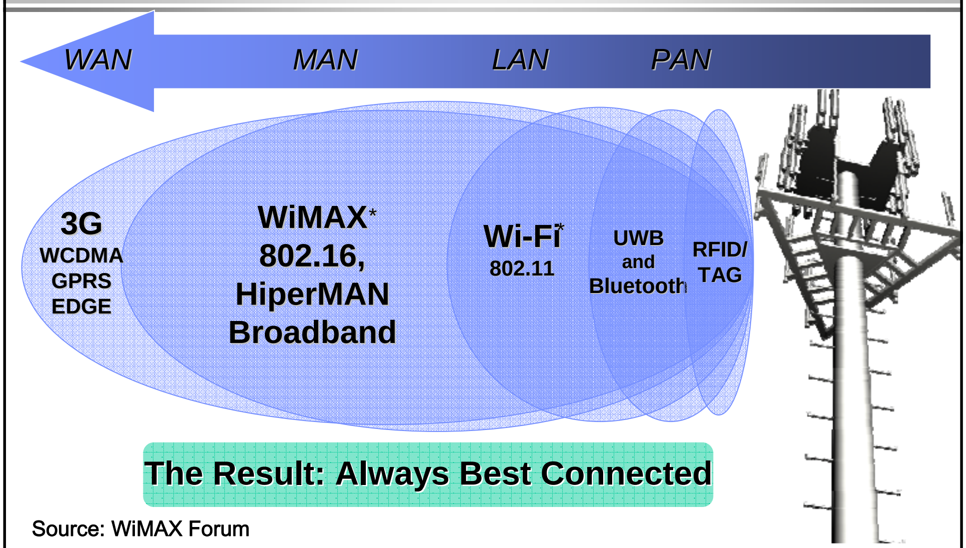
	802.16-2004	802.16e	HSDPA
Data Rate	75 Mbps/20MHz	15 Mbps/5MHz	14.4Mbps/5MHz
Cell Radius	5 km	5 km	2 km
Mobility	Portable	Up to 100 km/hr	Up to 120 km/hr
Freq. Allocation	2~11GHz	2~6GHz	1.9~2.2GHz
Spectral Efficiency	3.75 bps/Hz	3 bps/Hz	2.9 bps/Hz
Access Technology	OFDM	OFDM/OFDMA	CDMA
Modulation	BPSK, QPSK, 16QAM, 64QAM	BPSK, QPSK, 16QAM, 64QAM	BPSK, QPSK, 16QAM

The Comparison of Mobility



Reference Source：WiMAX Forum

Broadband Communication Network



Source: WiMAX Forum

Vision: Wireless Communication

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CMOS Wireless LAN Chip Design

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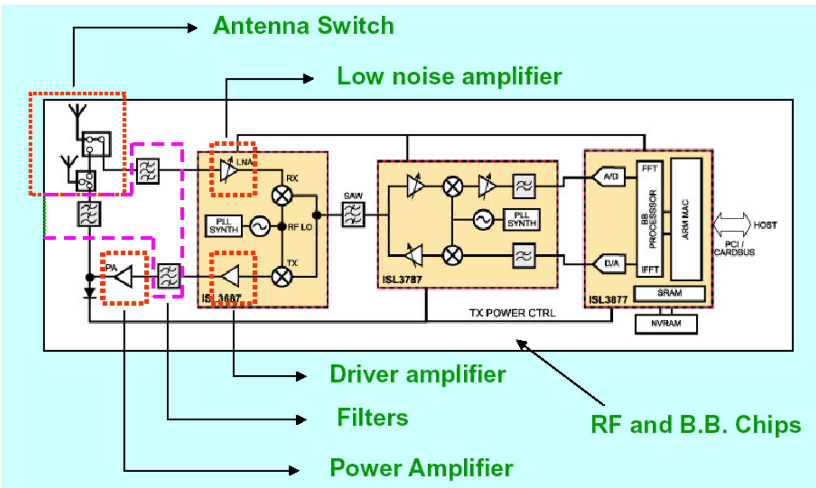
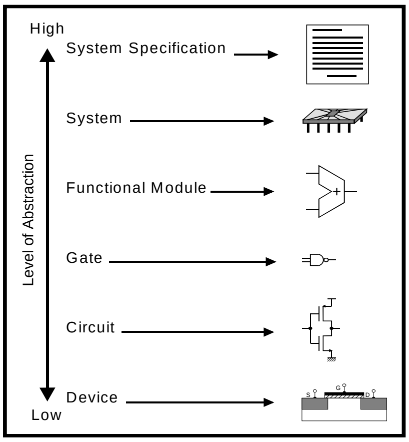
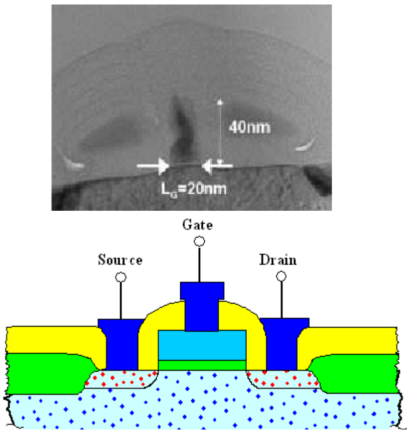


Design Abstraction Levels





CMOS Hierarchical Modeling and Design

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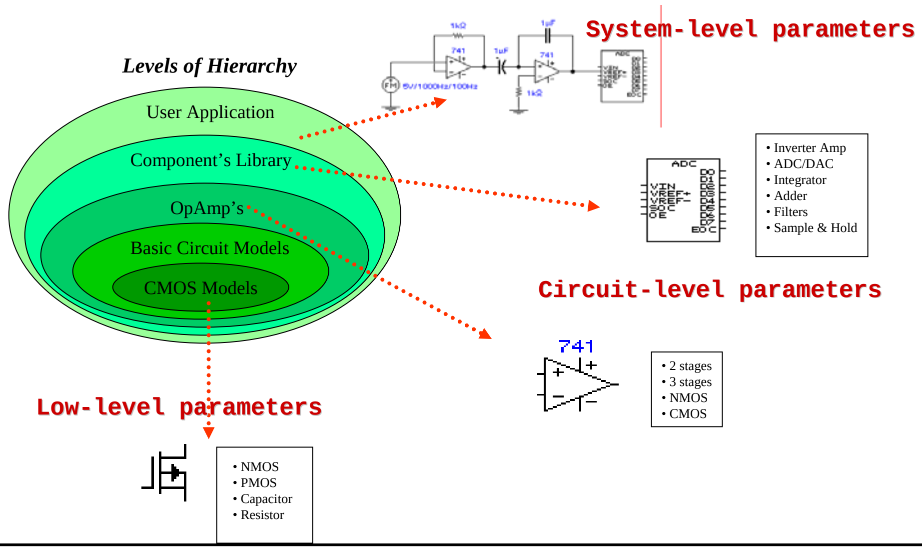
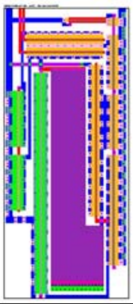


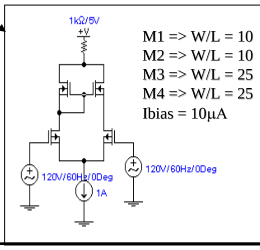
CMOS Analog Circuit Design Process

- ■Design Specifications.
- ■Topology Selection.
- ■Circuit Sizing.
- ■CMOS Layout.

Function:	Band Pass Pass Filter
Specifications:	BW = 50 KHz
	W_o = 679 Hz
	Pass Atten = -3dB
	Stop Atten = -10dB
Constraints:	Area = 1000 μm^2
	Power = 3 mW
	Zout = 300 ohms
	Gain = 4.5

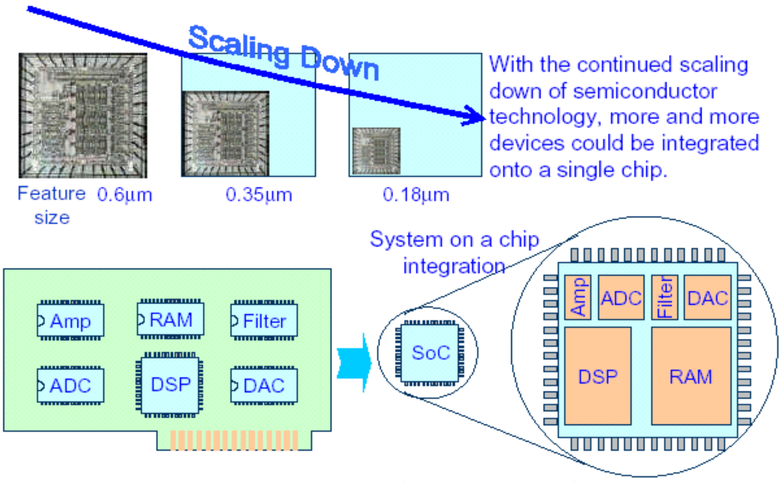
Style:	Butterworth
Order:	4th
Implementation:	Sallen-Key
Operational Amp:	3-stage CMOS





M1 => W/L = 10
M2 => W/L = 10
M3 => W/L = 25
M4 => W/L = 25
Ibias = 10µA

Mixed-Signal System-On-Chip Integration

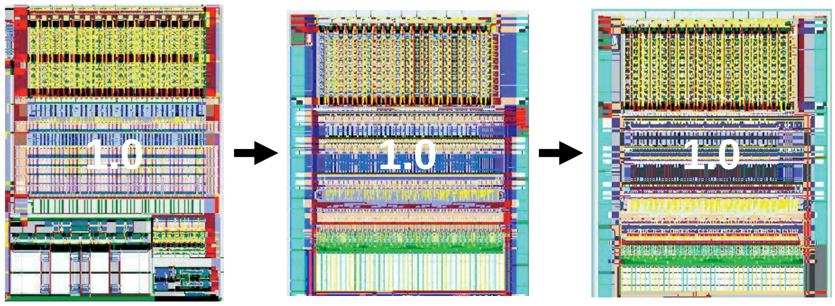


With the continued scaling down of semiconductor technology, more and more devices could be integrated onto a single chip.

Fig. 1.2, Mixed-signal system-on-a-chip integration

10-bit CMOS ADC Chip

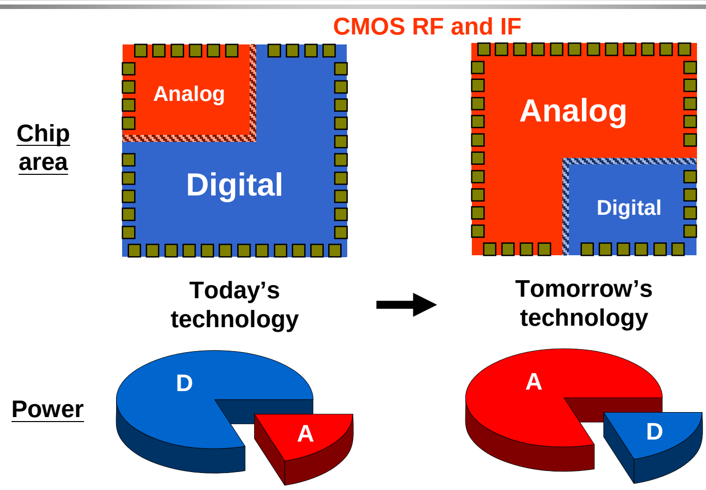
(Broadcom Corp.)



0.5μm, 5V **0.35μm, 3.3V** **0.25μm, 2.5V**

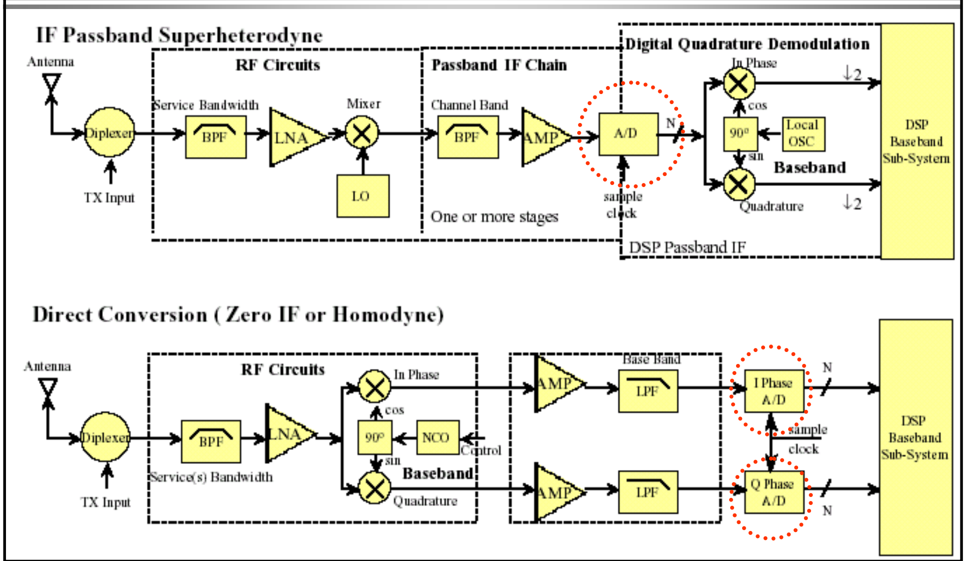
10-bit (Folding and Interpolating) ADC does not scale!

Impact of CMOS SoC Scaling



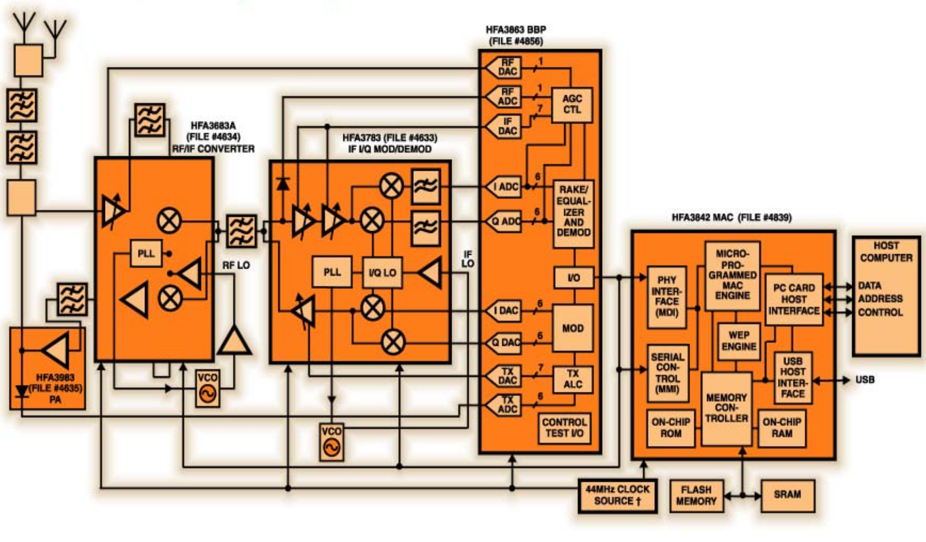
Cost dominated by Analog Circuit Design!

Communication Receiver Block Diagram



802.11 b WLAN Block Diagram

PRISM II, 11Mbps Chip Set Overview



† THE HFA3842 MUST BE SUPPLIED WITH A SEPARATE 48MHz CLOCK WHEN USB IS USED.

802.11a WLAN Block Diagram

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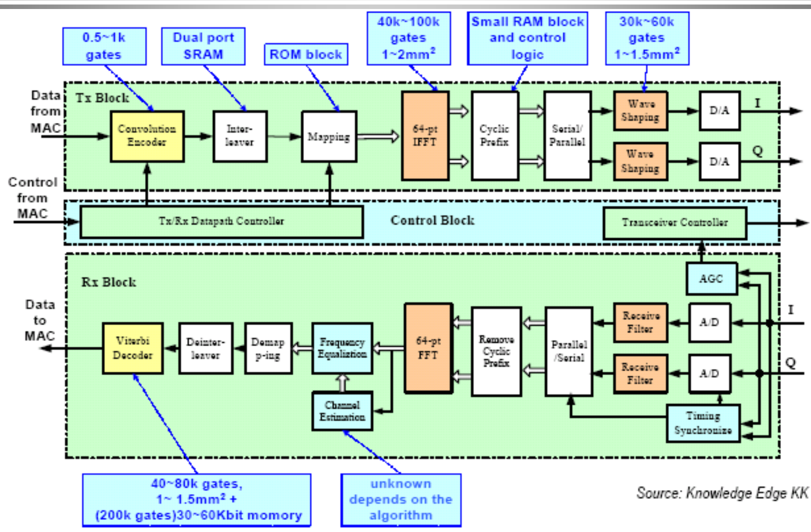

Source: Knowledge Edge KK

802.11a WLAN System Block Diagram

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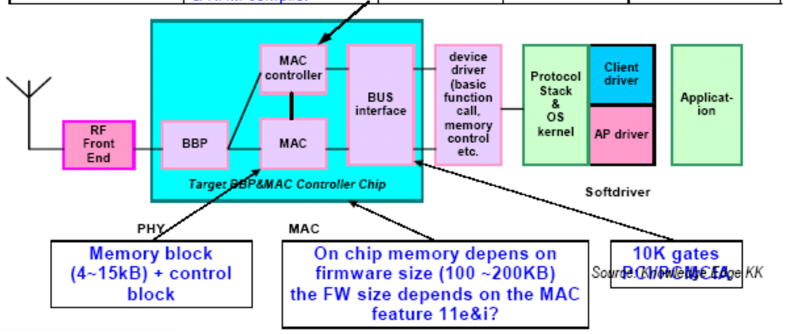
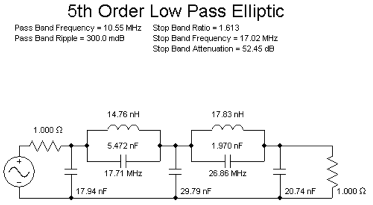
CPU core	Die area	Peak Power Consumption (mW/MHz)	Memory System	Clock frequency & MIPS performance
ARM9E / ARM946E-S cached processor with tightly coupled memory interfaces	4.9mm² on 0.18µm estimated size with 16KB instruction & 4KB data caches and no TCMs Using Artisan cell library & RAM compiler	1.1 mW/MHz @ 1.8V (estimated)	Selectable I & D cache sizes: 0, 4K, 8K... 1M Selectable I & D TCM sizes: 0, 4K, 8K... 1M	150MHz on TSMC 0.18µm (worst case) 230MHz on TSMC 0.18µm (typical)



Analog Filter Design

Analog Filter

●*Analog filter* uses analog electronic circuits from components, such as: resistors, capacitors and Inductors, to produce the required filtering effect.



●***Advantages*:**

- simple circuit design.
- fast and simple realization.

●***Disadvantages:***

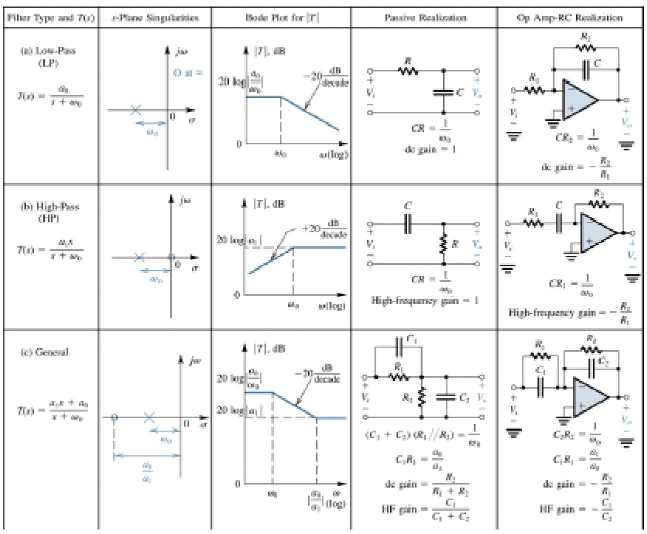
- Little stable and sensitive to temperature variations.
- Very expensive to realize in large amounts.
- Aged effect.
- Noise indued to Inductor.

Analog Filter Design Concept

Filter specifications → Continuous-Time Filter → Gm-C, Active RC-MOS-C or SC Filter Design

- ❑This *ideal* Filter specification cannot be achieve by realizable filters because an instantaneous transition from a gain of 1 to 0 is not possible.
- ❑Filter Synthesis: Synthesis is **generally not unique**. More than one circuit can satisfie H(s).
- ❑Today's Gm-C, Active-RC, MOS-C or switched capacitor filters are based on continuous time filters. Consequently, it is expedient to briefly review the subject of continuous time filters.
- ❑Gm-C, Active-RC, MOS-C or Switched Capacitor Filter *approximations* which closely approximate the ideal filter but are realizable.

First Order Filter

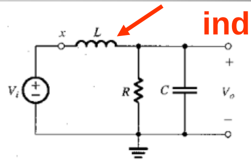


2nd Order LCR Resonators Circuit

Low-pass:

$$T(s)=a_2\frac{\omega_0^2}{s^2+s(\omega_0/Q)+\omega_0^2}$$

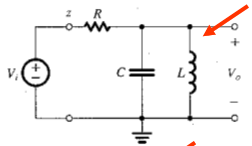
inductor L



Bandpass:

$$T(s)=a_2\frac{s(\omega_0/Q)}{s^2+s(\omega_0/Q)+\omega_0^2}$$

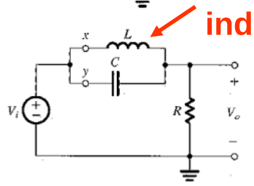
inductor L



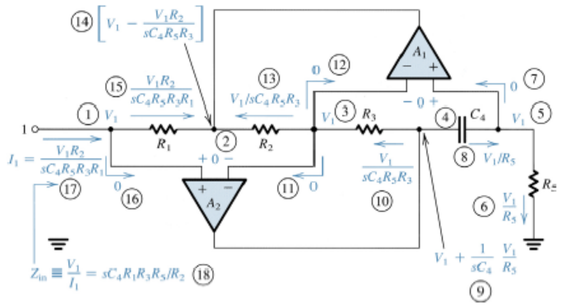
Notch:

$$T(s)=a_2\frac{s^2+\omega_0^2}{s^2+s(\omega_0/Q)+\omega_0^2}$$

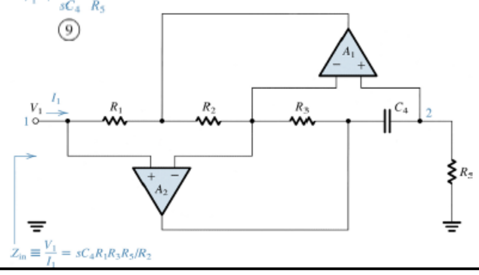
inductor L



Antoniou Inductance-Simulation Circuit Method



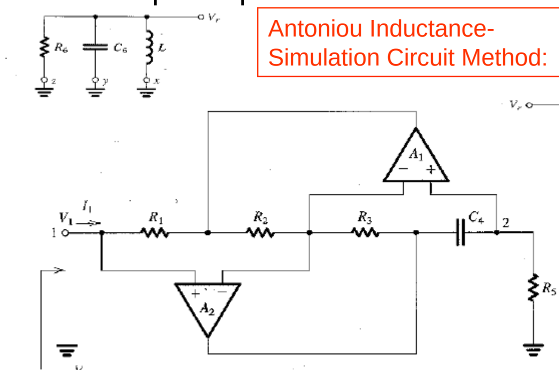
Begin

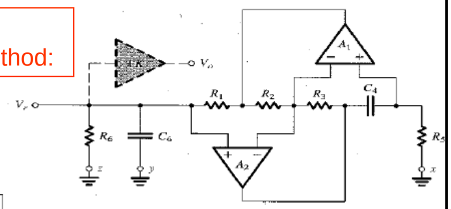


Second-Order Active Filter Design

■**Replace the inductor L :** by an op amp-RC circuit that has an inductive input impedance.

Antoniou Inductance-Simulation Circuit Method:

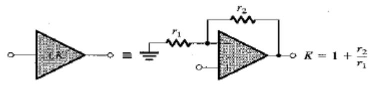




$Z_{in} \equiv \frac{V_1}{I_1} = sC_4R_1R_3R_5/R_2$

$L = C_4R_1R_3R_5/R_2$

Buffer Circuit Design



Continuous-time Anti-aliasing Filter Design

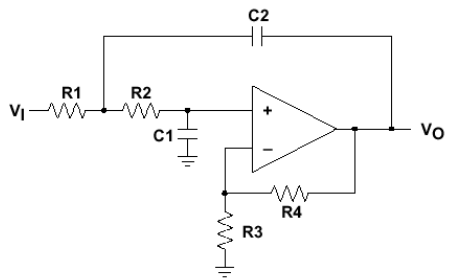


Figure 5. Low-Pass Sallen-Key Circuit

$$\frac{Vo}{Vi}(lp) = \frac{K}{s^2(R1R2C1C2) + s(R1C1 + R2C1 + R1C2(1-K)) + 1}$$

By letting

$$s = j2\pi f,\ fc = \frac{1}{2\pi\sqrt{R1R2C1C2}},\ \text{and } Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2(1-K)}.$$

參考 Project Report -5MHz CMOS Sallen-Key Low Pass Filter Circuits for DVB-H

Analog Continuous-Time Monolithic Filter

- ***Monolithic Filter*** : Low cost, good matching, reduce parasitic capacitance and automatic tuning for processing and temperature variation.
- Differential Equation from Laplace Transform: $s = j\,w$.
  - ⇒ Higher frequency response, lower power dissipation and area
  - ⇒ Lower Dynamic Range (DR).
- The standard active-RC filter: R,C and Op Amps with feedback loop.
- MOSFET-C filters : Op Amps and resistors often implemented with MOSFETs.
- Gm-C filters :resistors replaced by transconductors (used as open loop).
- Most straightforward design!

The Active-RC Filters

- **The drawbacks of Active-RC filters (R, C and Op Amp):**
  - ⇒ ***Smaller*** size than the passive filter (especially in low frequency).
  - ⇒ It is ***impossible*** to integrate the Resistor and Cap. into a Chip
    - for 1pf -> 2500 (50x50) um^2 (4 mil^2). 100pf ??

If : Voice band filter (0~4 KHz) :

RC= 10 krad/s, C = 10pf, R=10 MΩ -> 10^6 um^2 (1600 mil^2).

1. The *overall* chip area is around 20,000 mil^2 for this circuit.
2. The *Poly-Si* or Diffusion resistor is *nonlinear*.
3. The *error* of **resistor** is *10%*, and the *error* of **capacitor** is *10%*
   ⇒ The *error* of *RC* time constant is ***20% !***
4. The temperature and voltage coefficients of *RC* time constant are *not correlated and serious*.
   ⇒ *RC variation =~ 50% with fabrication process, temperature.*

- **The Active-RC and SC Filters are relatively mature technologies.**
- **The Active-Gm/C Filter offers potential applications up to VHF.**

Active-RC Filter

- Moderate-to-high frequency precision (with tuning).
  ⇒ Small area and low power dissipation for f<100 kHz.
- Feedback structure reduces sensitivity to parasitic.
- Can be realized as all biquad type circuits.

But:

- *On-chip tuning* and corresponding circuitry is required.
- Fully-balanced-differential structures for increasing linearity.
- Op Amps and feedback circuits limit the filter –3dB cutoff frequency. ⇐The RC time constant in Filter must be at most *5% or 10%* of Unity Gain bandwidth to avoid the pole frequency and quality factor error.
- Not suited for high-frequency applications !

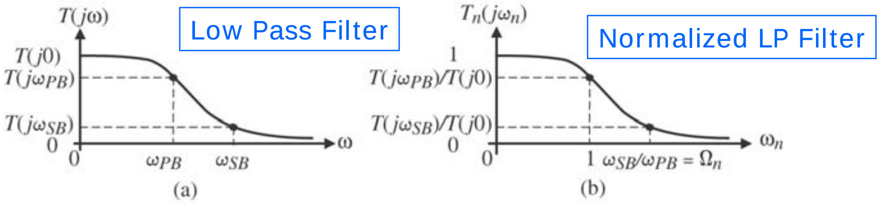
Filter Types

- Different types of polynomials :
  - ✓ Butterworth – smooth, well behaved, commonly used.
  - ✓ Chebyshev – faster roll-off but with ripple in either passband or stopband.
  - ✓ Elliptical – faster roll-off but with ripple in both passband and stopband.
  - ✓ Bessel- Approximately Linear Phase.

$$H(f) = \frac{a_0}{b_0 + b_1 s + \cdots + b_n s^n}$$

Characterization of Filter

❑A low pass filter magnitude response.



Three basic properties of filters.

1.) Passband ripple = $|T(j0) - T(j\omega_{PB})|$.

2.) Stopband frequency = ω_{SB}.

3.) Stopband gain/attenuation = $T(j\omega_{SB})$.

For a normalized filter the basic properties are:

1.) Passband ripple = $T(j\omega_{PB})/T(j0) = T(j\omega_{PB})$ if $T(j0) = 1$.

2.) Stopband frequency (called the transition frequency) = $\Omega_n = \omega_{SB}/\omega_{PB}$.

3.) Stopband gain = $T(j\omega_{SB})/T(j0) = T(j\omega_{SB})$ if $T(j0) = 1$.

Filter Specification by Bode Plot

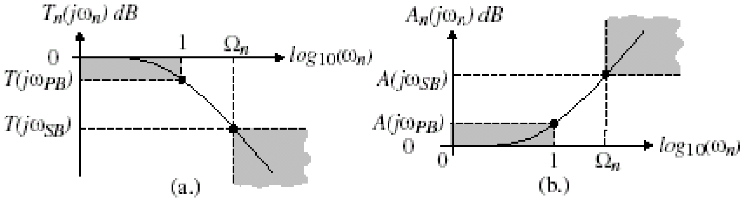


Figure 9.7-2 - (a.) Low pass filter of Fig. 9.7-1 as a Bode plot. (b.) Low pass filter of Fig. 9.7-2a shown in terms of attenuation ($A(j\omega) = 1/T(j\omega)$).

Therefore,

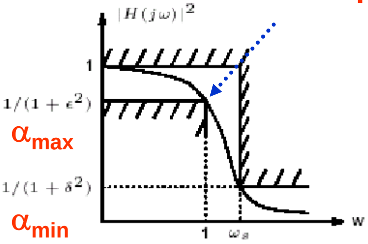
Passband ripple = $T(j\omega_{PB})$ dB

Stopband gain = $T(j\omega_{SB})$ dB or Stopband attenuation = $A(j\omega_{PB})$

Transition frequency is still = $\Omega_n = \omega_{SB}/\omega_{PB}$

Butterworth (Maximally Flat) Filter

-3dB cut-off frequency

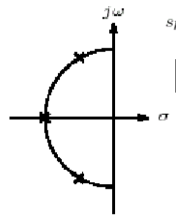


The transfer functions is

$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2\omega^{2N}}$$

N is the filter order, want **N: integer**

$$N \ge \frac{\log[(10^{0.1\alpha_{\max}}-1)/(10^{0.1\alpha_{\min}}-1)]}{2\log\omega_S}$$



The roots are at

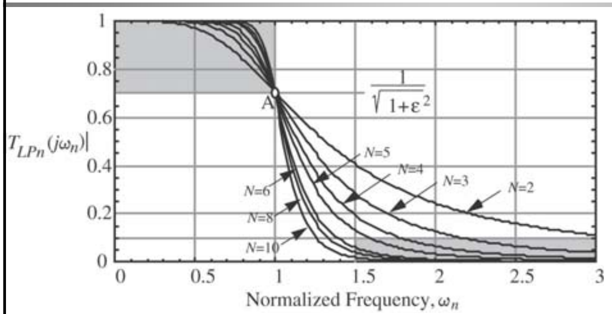
$$s_k = \epsilon^{-1/N} exp\left(j\frac{2k+N-1}{2N}\pi\right) \qquad k = 1, 2, \cdots, N$$

$$|H_n(j\omega)|^2 = \frac{1}{1+(s/j)^2} = \frac{1}{1+(-1)^n s^{2n}}$$

$$\theta_k = 90^o(\frac{2k+n-1}{n}) \quad k = 1,\ 2,\ ...,\ 2n$$

- Butter worth filter: many derivatives are zero at ω=0.
- All pole filter: **Good flatness in pass band.**
- **Poor phase linearity.**
- **Moderate attenuation slope steepness.**

Butterworth Filter Approximation



EXAMPLE 9.7-1: Determining the Order of A Butterworth Filter Approximation

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1+\varepsilon^2\,\omega_n^{2N}}}$$

where N is the order of the approximation and ε is defined in the above plot.

The magnitude of the Butterworth filter approximation at ω_{SB} is given as

$$\left|T_{LPn}\left(\frac{j\omega_{SB}}{\omega_{PB}}\right)\right| = |T_{LPn}(j\Omega_n)| = T_{SB} = \frac{1}{\sqrt{1+\varepsilon^2\,\Omega_n^{2N}}}$$

This equation in terms of dB is useful for finding N given the filter specifications.

$$20\ log_{10}(T_{SB}) = T_{SB}\ (dB) = -10\ log_{10}\left(1+\varepsilon^2\,\Omega_n^{2N}\right)$$

Poles and Quadratic Factors of Normalized LP Butterworth Function

Table 9.7-1 - Pole locations and quadratic factors ($s_n^2 + a_1 s_n + 1$) of normalized, low pass Butterworth functions for $\varepsilon = 1$. Odd orders have a product (s_n+1).

N	Poles		a_1 coefficient	
2	-0.70711 ± j0.70711		1.41421	
3	-0.50000 ± j0.86603		1.00000	
4	-0.38268 ± j0.92388 -0.92388 ± j0.38268		0.76536 1.84776	
5	-0.30902 ± j0.95106 -0.80902 ± j0.58779		0.61804 1.61804	
6	-0.25882 ± j0.96593 -0.70711 ± j0.70711	-0.96593 ± j0.25882	0.51764 1.41421	1.93186
7	-0.22252 ± j0.97493 -0.62349 ± j0.78183	-0.90097 ± j0.43388	0.44505 1.24698	1.80194
8	-0.19509 ± j0.98079 -0.55557 ± j0.83147	-0.83147 ± j0.55557 -0.98079 ± j0.19509	0.39018 1.11114	1.66294 1.96158
9	-0.17365 ± j0.98481 -0.50000 ± j0.86603	-0.76604 ± j0.64279 -0.93969 ± j0.34202	0.34730 1.00000	1.53208 1.87938
10	-0.15643 ± j0.98769 -0.45399 ± j0.89101 -0.70711 ± j0.70711	-0.89101 ± j0.45399 -0.98769 ± j0.15643	0.31286 0.90798 1.41421	1.78202 1.97538

Chebyshev Filter

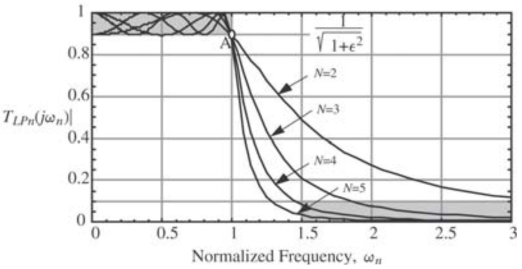


Figure 9.7-5

The magnitude of the normalized, Chebyshev, low-pass, filter approximation can be expressed as

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1 + \varepsilon^2 cos^2[Ncos^{-1}(\omega_n)]}} \quad , \quad \omega_n \le 1$$

and

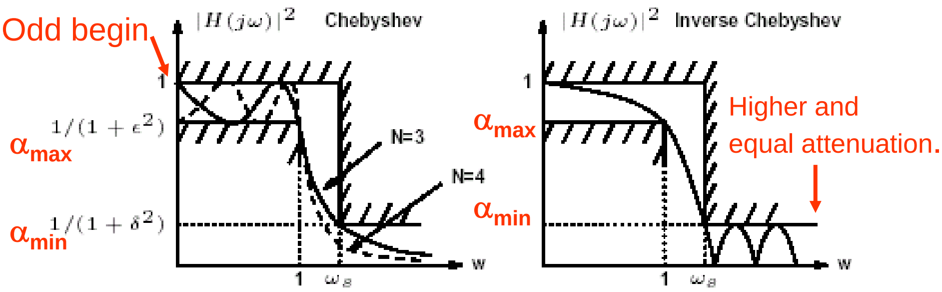
$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1 + \varepsilon^2 cosh^2[Ncosh^{-1}(\omega_n)]}} \quad , \quad \omega_n > 1$$

where N is the order of the filter approximation and ε is defined as

$$|T_{LPn}(\omega_{PB})| = |T_{LPn}(1)| = T_{PB} = \frac{1}{\sqrt{1+\varepsilon^2}}.$$

N is determined from $20\, log_{10}(T_{SB}) = T_{SB}(dB) = -10 log_{10}\{1 + \varepsilon^2 cosh^2[Ncosh^{-1}(\Omega_n)]\}$

Chebyshev (Equip-Ripple) Filter



- **Distribute the magnitude error in the passband or stopband.**

Chebyshev

$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2 C_N^2(\omega)}$$

Inverse Chebyshev

$$|H(j\omega)|^2 = \frac{\epsilon^2 C_N^2(1/\omega)}{1+\epsilon^2 C_N^2(1/\omega)}$$

- **Less order N than Butterworth filter (due to sharper TB).**

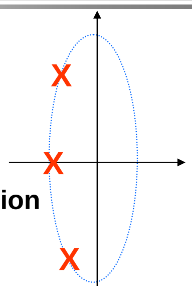
Chebyshev Filter

Chebyshev Polynomial :

$$\begin{aligned} C_N(\omega) &= \cos[N\cos^{-1}(\omega)] \quad \text{for} \quad \omega \le 1 \\ &= \cosh[N\cosh^{-1}(\omega)] \quad \text{for} \quad \omega > 1 \\ &= 2\omega C_{N-1}(\omega) - C_{N-2}(\omega) \end{aligned}$$

N is the filter order, want

$$N \ge \frac{\cosh^{-1}(\delta/\epsilon)}{\cosh^{-1}\omega_s} \approx \frac{\ln(2\delta/\epsilon)}{\ln\left(\omega_s + \sqrt{\omega_s^2 - 1}\right)}$$



•Ellipse
Pole location

$$\left(\frac{\sigma_k}{\sinh a}\right)^2 + \left(\frac{w_k}{\cosh a}\right)^2 = 1$$

$$Q_k = w_k / 2\sigma_k$$

- **Good steepness of the attenuation slope.**
- **Poor phase linearity (delay distortion), and pass band flatness.**
- **Inverse Chebyshev filters (with transmission zeros in the stop band): have better phase and lower Q (but less sensitive to component tolerance).**

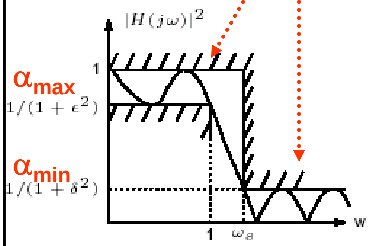
Poles and Quadratic Factors of Normalized LP Chebyshev Function

Table 9.7-2 - Pole locations and quadratic factors ($a_0 + a_1 s_n + s_n^2$) of normalized, low pass Chebyshev functions for $\varepsilon = 0.5088$ ($1dB$).

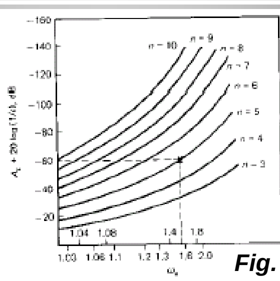
N	Normalized Pole Locations	a_0	a_1
2	-0.54887 ± j0.89513	1.10251	1.09773
3	-0.24709 ± j0.96600 -0.49417	0.99420	0.49417
4	-0.13954 ± j0.98338 -0.33687 ± j0.40733	0.98650 0.27940	0.27907 0.67374
5	-0.08946 ± j0.99011 -0.23421 ± j0.61192 -0.28949	0.98831 0.42930	0.17892 0.46841
6	-0.06218 ± j0.99341 -0.16988 ± j0.72723 -0.23206 ± j0.26618	0.99073 0.55772 0.12471	0.12436 0.33976 0.46413
7	-0.04571 ± j0.99528 -0.12807 ± j0.79816 -0.18507 ± j0.44294 -0.20541	0.99268 0.65346 0.23045	0.09142 0.25615 0.37014

Elliptic (Cauer) Filter

transmission zeros



Narrower TB



20log Rn(ω_s)

α_{min} =50dB

ω_s=1.5

ε=0.5dB.

***N* = 5**

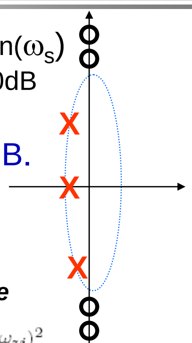


Fig. 8.16 Design curve

The transfer functions is

$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2 R_N^2(\omega)}$$

where

$$R_N(\omega) = k\prod_{i=1}^{N/2}\frac{\omega^2-(\omega_s/\omega_{zi})^2}{\omega^2-\omega_{zi}^2} \quad \text{for } N \text{ even}$$

$$= k\omega\prod_{i=1}^{(N-1)/2}\frac{\omega^2-(\omega_s/\omega_{zi})^2}{\omega^2-\omega_{zi}^2} \quad \text{for } N \text{ odd}$$

$$\alpha_{\min} = 10\log[1+\varepsilon^2 R^2{}_n(\omega_s)]$$

- ***Best steepness*** **of the attenuation slope.**
- **Complex elliptic function *(by MATLAB)*.**
- **Poor phase linearity.**

In the stopband, if $\epsilon^2 R_N^2(\omega) \gg 1$,

$$20\log\frac{\delta}{\epsilon} \approx 20\log|R_N(\omega_s)|$$

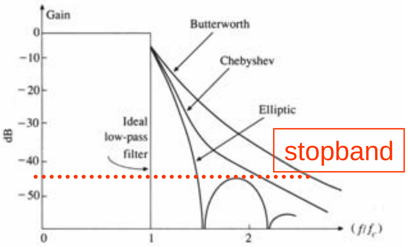
Comparison of Classical Filter

❑ α_{max}= 0.5dB, ω_p= 15.9 KHz, α_{min} = 50 dB, ω_s / ω_p =1.5 ⇒Butterworth n=17, Chebyshev n =8, Elliptic filter n =5 (due to the narrower TB).

❑ **Order :** α_{max}= 0.25dB, ω_p= 100 Krad/s, α_{min} = 18 dB, ω_s = 140 Krad/s ⇒Butterworth n=11, Chebyshev n =5, Elliptic filter n =4.

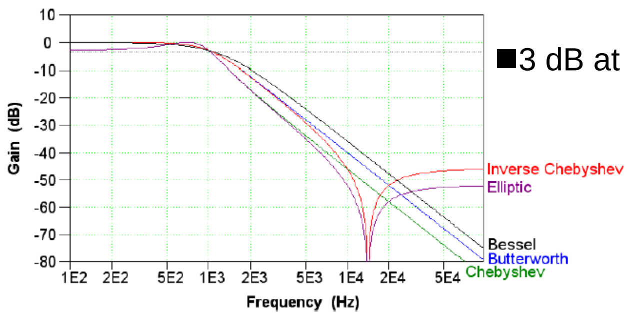
❑**Q-value :**
α_{max}= 0.25dB, α_{min} = 18 dB, n=5, $Q_C > Q_{IC}$.

$$Q^2{}_C = 1.573 Q^2{}_{IC} - 0.1434$$



❑**Circuit realization :** Generally, the order of Analog active filter N is limited below 10. The order is better in the range of 4 ~ 6.

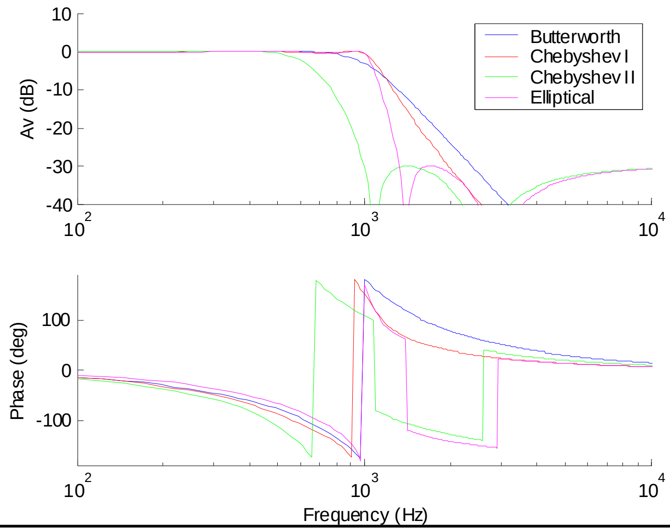
Comparison of Classical Low Pass Filter



■3 dB at the 10 kHz.

■Butterworth is the most popular response. It has no ripple in the pass or stop.
■Chebyshev response has more roll off than Butterworth.
■Inverse Chebyshev response has ripple in the stop band, and therefore has a lot of rejection near the corner frequency, but the rejection bounces back, and there is some passage in the stop band.
■Elliptical response combines the characteristics of Chebyshev and inverse Chebyshev, having ripple in the pass band and in the stop band. Like the inverse Chebyshev, the stop band rejection has some bounce back.
■Bessel response has less rolloff in the stop band than the other types, and is not as flat in the pass band.

Transfer functions of different filter types (all 4th order)

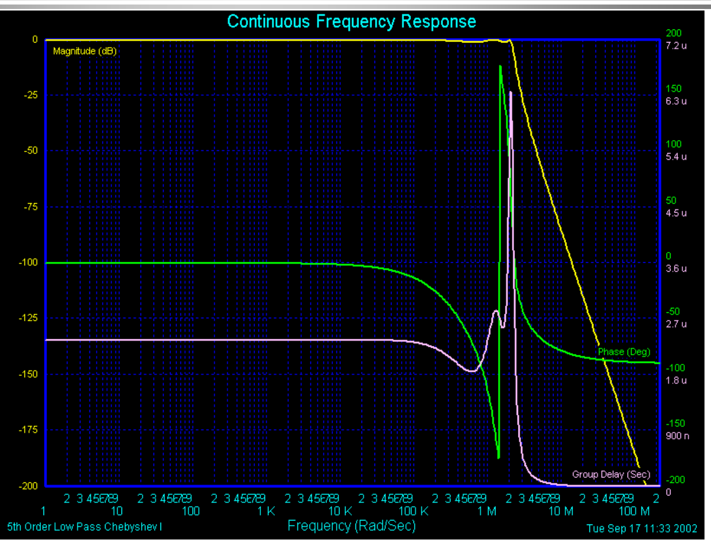


LP Filter Response : 2MHz

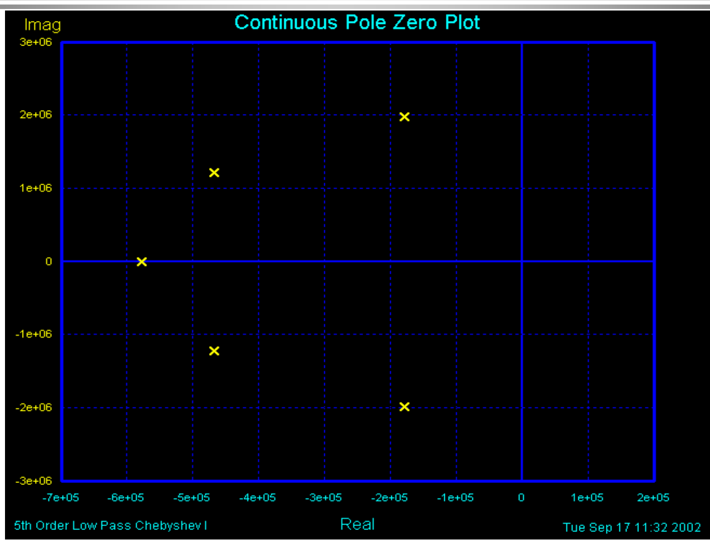
Magnitude:

Phase

Group Delay



LP Filter : Poles and Zero



Biquad and Ladder Filter Design

- **Biquad filters : Sensitivity and Noise in key issue.**
  - ✓ **Higher sensitivity of component variations.**
  - ✓ **Easier to compute - divide problem into subproblems (cascade-second order filters such as: Butterworth, Chebyshev, Elliptic (Cauer) and Bessel (linear Phase) etc.).**
  - ✓ **Active elements : R, C and Op Amp.**
  - ✓ **5th orderBiquad : 1st + Hi-Q + Low-Q**
  - ✓ **6th orderBiquad : Hi-Q + Mid-Q + Low-Q**
  - ✓ **SCF, Gm-C Filter.**
- **Ladder filters : Good choice!!**
  - ✓ **Low sensitivity to component variations.**
  - ✓ **Not Easy to compute – by Table filters such as: Butterworth, Chebyshev, Elliptic (Cauer) and Bessel (linear Phase) etc.**
  - ✓ **Passive elements such as : R, L and C.**
  - ✓ **SCF, Gm-C Filter.**

Digital Filter

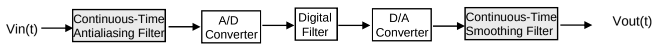
- Digital Filters : DSP

⇒Discrete time system by Difference Equation.

⇒ A/D introduces quantization noise.

⇒ Z-transform, Z^{-1} is the unity delay.

⇒ With Programmability and larger Dynamic Range (DR).



Switched Capacitor Filter Design

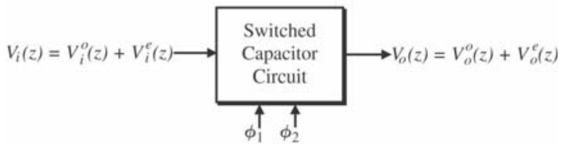
The Concept of SC Networks

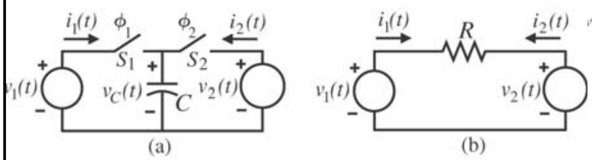
- **The most popular approach in analog signal processing since early 1970.**
- **Compatibility with standard CMOS process technologies.**
- **No A/D and D/A converters** ⇒***Analog Sampled Data (Discrete time signal) system with DSP concept.***
- **Accurate discrete-time frequency (0.1%)** ⇒ **since the** *Filter coefficients (time constant)* **determined by** *Capacitor Ratio and clock (sampling) frequency.*
- **Very Good voltage linearity.**
- **Good Process and Temperature characteristics.**
- Switched Capacitor Network's (SCN) main Applications :
  - ✓ Filter, ADC and DAC, Sigma-Delta Modulators, Gain-stages in DAC, Voltage-Control Oscillators, Decimation and Interpolation Filter.

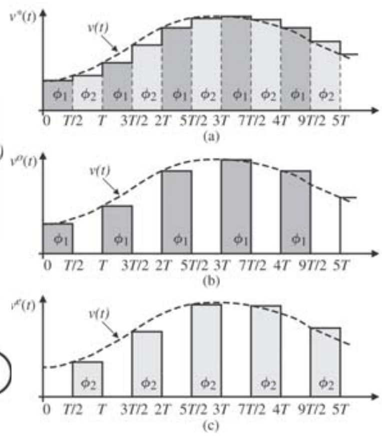
Switched Capacitor Circuits

Sampled-data Signal:

Continuous amplitude, discrete time signal.

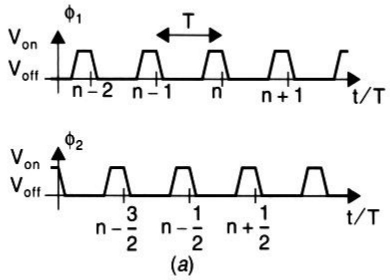






Resistor Emulation!

Basic Switched Circuits Concept



- SC simulated **Positive** resistor :

$\phi_1: V_{c1} = V_1 \quad \phi_2 : V_{c1} = V_2$

=> $\Delta Q = C\,(V_1 - V_2)$

$f_s \equiv \frac{1}{T}$ Equivalent average current in each clock :

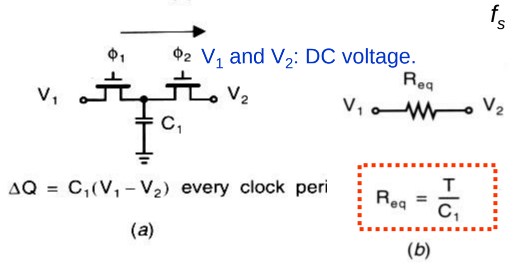
$\Delta Q/T = i_{avg} = C(V_1 - V_2)/T = C\,f(V_1 - V_2) = (V_1 - V_2)/R$

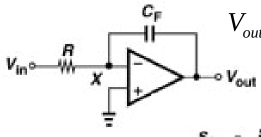
=> $\boxed{Req = T/C = 1/(Cf_s)}$ f_s :clock frequency.

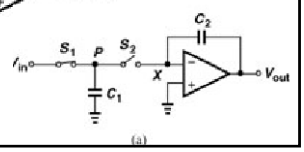
- Example 9.1-1 : Allen's Book

f_s =100 KHz, C=10pf => R=1 M Ω , less area .

$$V_{out} = -\frac{1}{RC_F}\int V_{in}\,dt$$



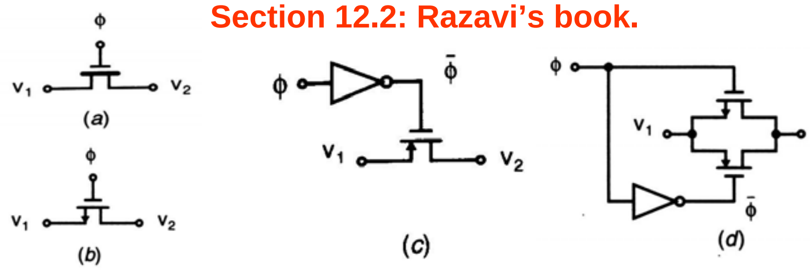




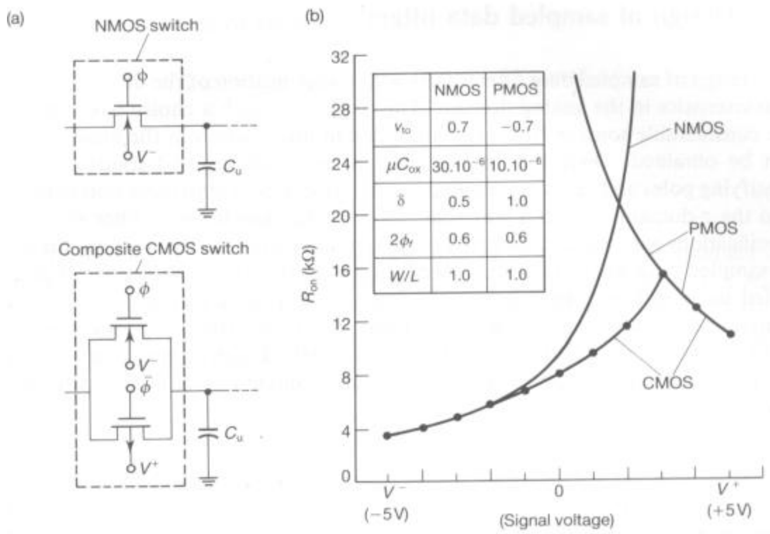
CMOS Switches

- **NMOS** or **PMOS** switch only ⇒**V1 or V2 (=** V_{DD}**-**V_{tn} =0 ~ 4 v) due to the body effect or (= V_{DD}-V_{tp} =1 ~ 5 v). ⇒ **CMOS** switch.
- **CMOS** switch can cancel the nonlinear effects from Nonlinear parasitic cap, channel charge injection, clock feed through, Noise and capacitive coupling from logic signal to each side of the CMOS switch.

Section 12.2: Razavi's book.

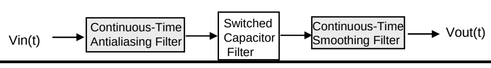


On-resistance in CMOS Switch circuits



Switched Capacitor Filter

- Switched Capacitor (Sampled-Data) Filters : Discrete (sampled) time but continuous (analog) in amplitude.
  - ✓ Resistors replaced by switched capacitors.
  - ✓ Parasitic Capacitance insensitive.
  - ✓ Very high precision without tuning.
  - ✓ Fully-balanced-differential structures for high dynamic range (DR).
  - ✓ Small area and low power dissipation.
- Much more widely used!



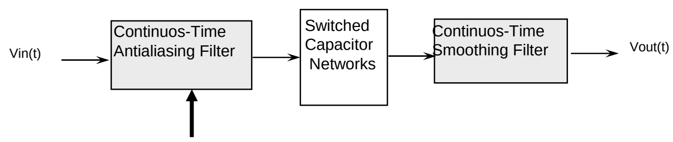
Basic Concepts of SCF

- **General Switched Capacitor Networks (SCNs)** :
- **Ideal capacitors, ideal voltage-controlled voltage sources (VCVS), ideal switches and sampled-data voltage inputs**.
- **VCVS ⇒ Freq. indep. gain amps or infinite gain Op Amp.**

⇒ Typically, the sampled-data voltage inputs is only single, not multiple.

⇒ The input may be a continuous or Sampled-and-Hold (S/H) signal.

⇒ The voltages of nonideal switches, non-ideal OP AMPs, non-ideal cap. should be considered as *second order* effects.



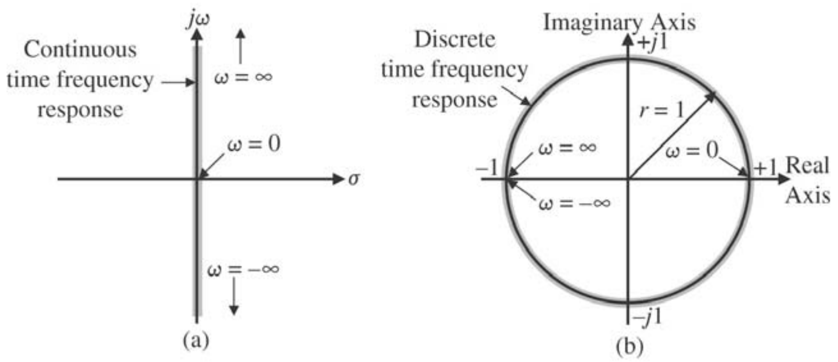
Sallen-Key Low-Pass Filter

Switched Capacitor Filter

- Switched Capacitor (Sampled-Data) Filters : Discrete (sampled), But:
  - ✓ Needs clock circuits.
  - ✓ Sample-data effects : Needs Anti-aliasing Filter required to prevent the high frequency signal input.
  - ✓ Reconstruction (smoothing) filter is required to smoothen the staircase signal and high frequency noise.
  - ✓ S-to-Z-transform by Bilinear and LDI (Realize functions with no CT equivalent)
  - ✓ Inefficient use of Op Amp's bandwidth: f_{cutoff}/ *Fs* >> 1 *for Sinc(x)=**sin(x) /x** (Sampled/Hold) Effect*.
  - ✓ Not suited for high-frequency applications (less than 50MHz LP Filter).

The s-z Transformation

$Z = re^{jwt}$

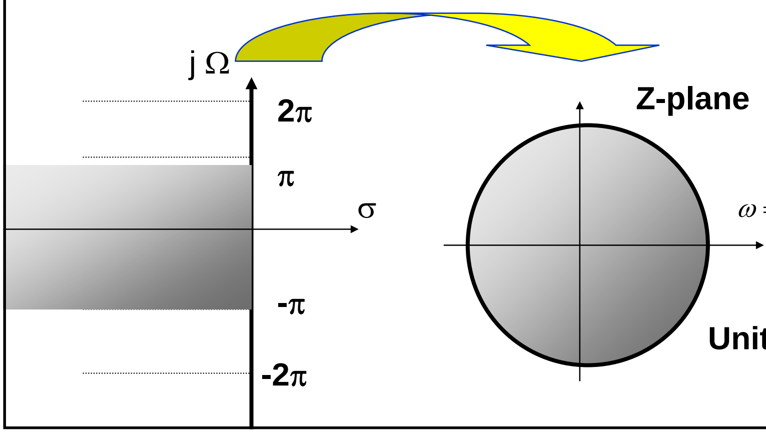


The LDI s-z Transform Method

- The LDI-z transformation (midpoint integration):

⇒ Warping effect (frequency axis expand)!

⇒ Approximately design the LC ladder filter.



$$s \leftrightarrow \frac{z^{1/2} - z^{-1/2}}{T}$$

$$\omega = \frac{2}{T}\sin(\frac{\Omega T}{2})$$

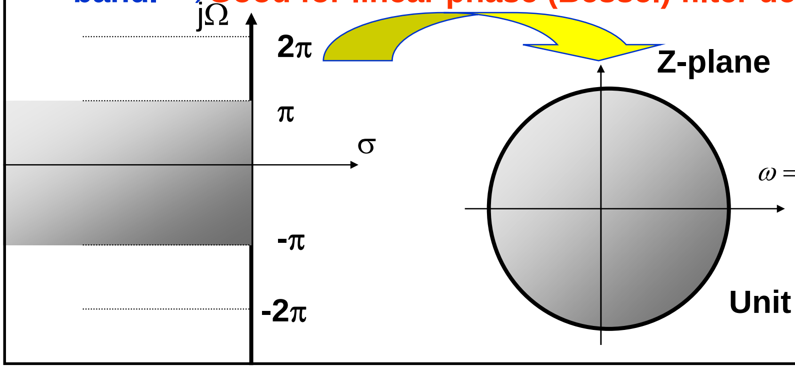
The Bilinear s-z Transform Method

- **The Bilinear-z transformation :**

⇒ Warping effect (frequency axis shrink)!

⇒ Exactly design the LC ladder filter.

- **Preserve both the loss and phase response in pass band. ⇒ Good for linear phase (Bessel) filter design!**



$$s \leftrightarrow \frac{2}{T}\frac{z-1}{z+1}$$

$$\omega = \frac{2}{T}\tan\left(\frac{\Omega T}{2}\right)$$

The s-z LDI and Bilinear Transform

•If Input signal frequency f <<Fs sampling frequency

⇒ No need of *sinx/x* compensation and *prewarping*.

•However, The LDI or Bilinear Transformation have the *phase error* due to the frequency-axis warping.

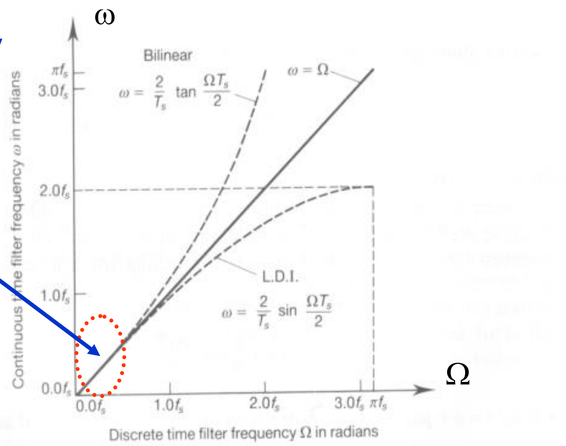
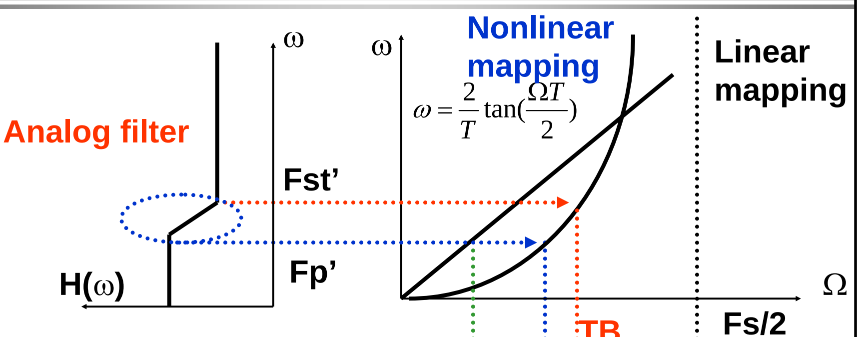
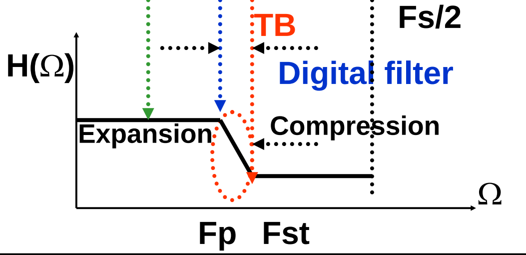


Fig. 1.15 Warping effect introduced by bilinear and LDI transformations *(adapted from*

Frequency-Axis Warping of Bilinear Transform

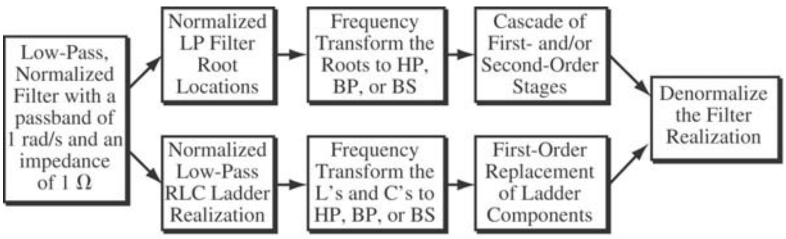




•If the filter band edge near sampling frequency Fs
⇒ The band edge need frequency-axix *prewarping*.

Higher-order Filter Design : Cascade Approach

Higher-order Filter Design



❑*Cascade Approach: Simpler* Z-domain digital Filter synthesizer (Design according to the filter spec. and sampling frequency).

Issues:

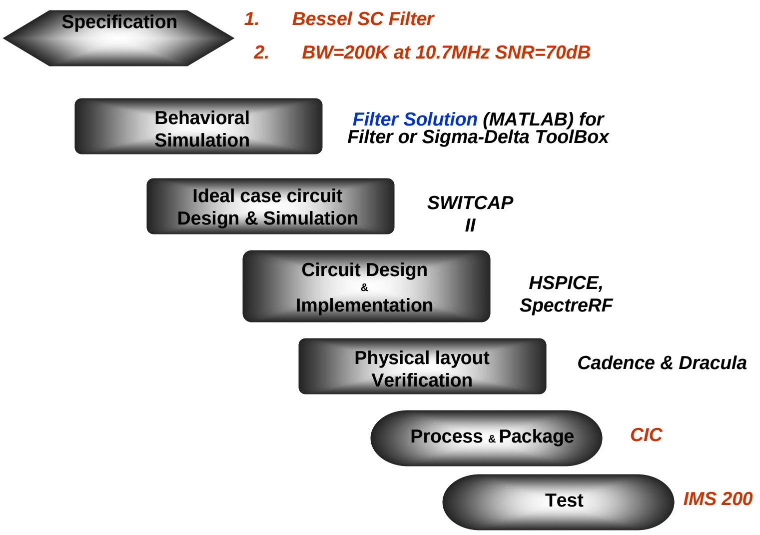
1. **Higher** Filter coefficient **sensitivity structure.**
2. **The Coefficient arrangement in each block.**
3. **Noise problems.**

Z-domain digital Filter :

FDS Synthesizer by SPW

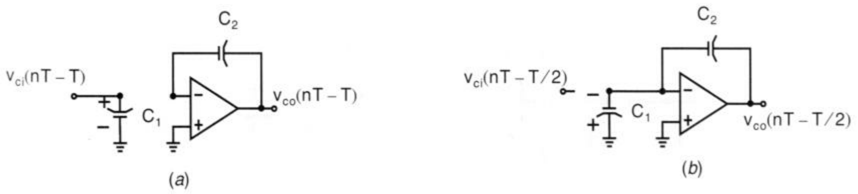
- *Simpler* Z-domain digital Filter synthesizer (according to the filter spec. and sampling frequency). ⇐However, this architecture will have higher Filter coefficient sensitivity.
- The biquadratic circuit's H(z) for 6^{th} order **(2-2-2)** or 5^{th} order **(1-2-2)** can be designed in the Z-domain directly (choose the Chebyshev, Elliptic, Bessel filter type) in *SPW or Matlab*.
- Realized (Synthesized) the Z-domain coefficients by the capacitor's ratio of SC biquadratic circuits such as Laker's SC blocks from H(z).
- Simulated again by SWITCAP II for spec. checking (include the dynamical capacitor scaling in each op amp output, and minimum capacitor scaling in each virtual GND.
- Overall SC mixed-signal circuits layout (Be careful in choosing unit capacitor, Cu).

SCF Design Flow

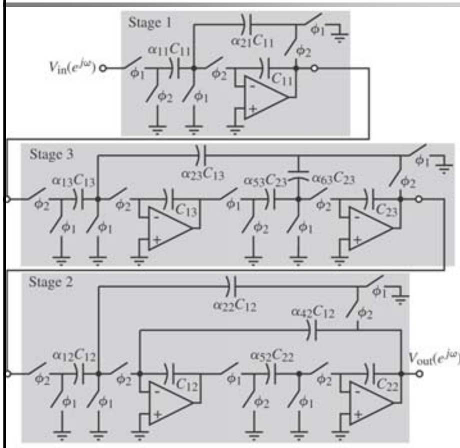


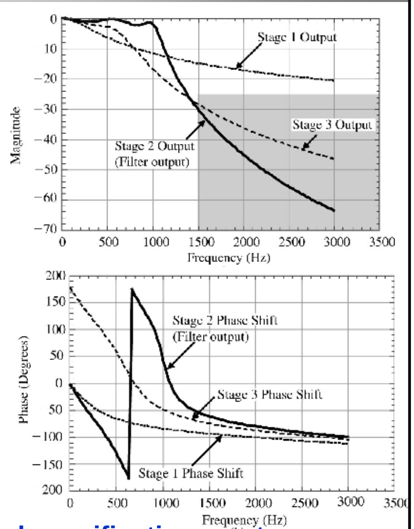
Simulation of SC circuits

- SCN is a LTV (Linear Time Varying) system and not easily simulated by **HSPICE** for **frequency response.**
- SCN is a Linear System with less HD.
- SC integrator **approximates** the ideal continuous-time integrator when the input frequency is much less than the sampling frequency.
- **HSPICE case : This tool is not a good simulation method!** (Example 9.7-5 Allen's book, page 541, 569~580) so you better use **SWITCAP II and SpectreRF.**



5th-order Chebyshev LP Filter Design





•There appears to be a sinx/x effect on the magnitude which causes the passband specification to not be satisfied. **•Stopband specifications met**

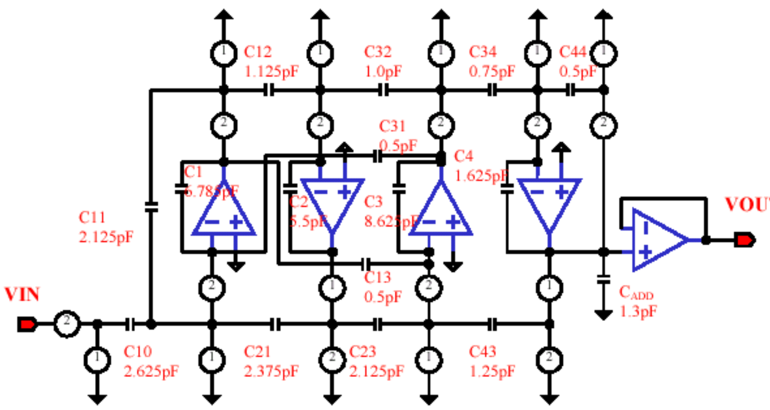
5^{th}-order Chebyshev LP Filter Design

Switcap2 Input File (The exact same results were obtained as for SPICE)

```
TITLE: EXAMPLE 9-7-5

OPTIONS;
 NOLIST;
 GRID;
 END;

TIMING;
 PERIOD 50E-6;
 CLOCK CLK 1 (0 25/50);
 END;

SUBCKT (1 100) STG1;
 S1     (1 2)       CLK;
 S2     (2 0)       #CLK;
 S3     (3 4)       #CLK;
 S4     (3 0)       CLK;
 S5     (5 100)     #CLK;
 S6     (5 0)       CLK;
 CL11   (2 3)       0.0909;
 CL21   (3 5)       0.0909;
 E1     (100 0 0 4) 1E6;
 END;

SUBCKT (200 300) STG2;
 S1     (200 2)     #CLK;
 S2     (2 0)       CLK;
 S3     (3 0)       CLK;
 S4     (3 4)       #CLK;
 S5     (6 5)       CLK;
 S6     (6 0)       #CLK;
 S7     (7 0)       CLK;
 S8     (7 8)       #CLK;
 S9     (300 9)     #CLK;
 S10    (9 0)       #CLK;
 CL12   (2 3)       0.3123;
 CL22   (3 9)       0.3123;
 CL42   (4 300)     0.1799;
 C12    (4 5)       1;
 CL52   (6 7)       0.3123;
 C22    (8 300)     1;
 E1     (5 0 0 4)   1E6;
 E2     (300 0 0 8) 1E6
 END;

SUBCKT (100 200) STG3;
 S1     (100 2)     #CLK;
 S2     (2 0)       CLK;
 S3     (3 0)       CLK;
 S4     (3 4)       #CLK;
 S5     (6 5)       CLK;
 S6     (6 0)       #CLK;
 S7     (7 0)       CLK;
 S8     (7 8)       #CLK;
 S9     (200 9)     #CLK;
 S10    (9 0)       #CLK;
 CL13   (2 3)       0.2058;
 CL23   (3 9)       0.2058;
 CL63   (9 7)       0.1471;
 C13    (4 5)       1;
 CL53   (6 7)       0.2058;
 C23    (8 200)     1;
 E1     (5 0 0 4)   1E6;
 E2     (200 0 0 8) 1E6
 END;

CIRCUIT;
 X1     (1 100)     STG1;
 X2     (100 200)   STG3;
 X3     (200 300)   STG2;
 V1     (2 0);
 END;

ANALYZE SSS;
 INFREQ 1 3000 LIN 150;
 SET V1 AC 1.0 0.0;
 PRINT vdb(100) vp(100);
 PRINT vdb(200) vp(200);
 PRINT vdb(300) vp(300);
 PLOT vdb(300);
 END;

END;
```


Micropower Low Pass Ladder Filter Simulation - Circuit and Input Description


```
TITLE: Switch Capacitor Low-pass Filter
 TIMING;
 PERIOD 1E-5;
 CLOCK CLK 1 (0 1/2);
END;

CIRCUIT;
S1  (1 2) #CLK;
S2  (2 0) CLK;
S3  (3 0) CLK;
S4  (4 0) #CLK;
S5  (5 0) CLK;
S6  (6 0) #CLK;
S7  (3 7) #CLK;
S8  (4 19) CLK;
S9  (5 9) #CLK;
S10 (6 10) CLK;
S11 (8 14) #CLK;
S12 (14 0) CLK;
S13 (11 15) #CLK;
S14 (15 0) CLK;
S15 (12 16) #CLK;
S16 (16 0) CLK;
S17 (13 17) #CLK;
S18 (17 0) CLK;
S19 (18 10) #CLK;
S20 (18 0) CLK;
C1  (2 3) 2.625;
C2  (3 4) 2.375;
C3  (4 5) 2.125;
C4  (5 6) 1.25;
C5  (3 14) 2.125;
```

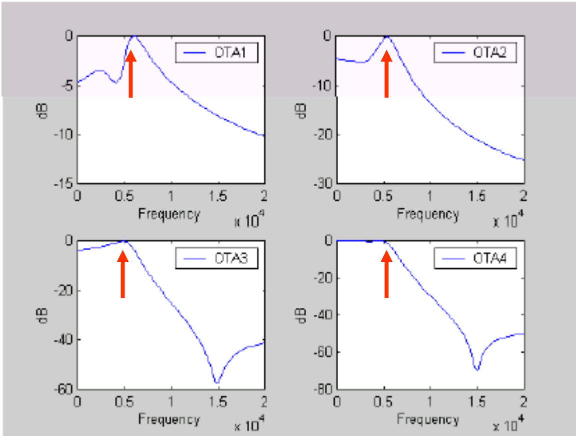


Low Pass Ladder Filter Simulation Result

2010/5/3

Ron-Yi Liu

```
C6  (7 8) 6.875;
C7  (19 11) 5.5;
C8  (9 12) 8.625;
C9  (10 13) 1.625;
C10 (10 0) 1.3;
C11 (14 15) 1.125;
C12 (15 16) 1.0;
C13 (16 17) 0.75;
C14 (17 18) 0.5;
C15 (7 12) 0.5;
C16 (8 9) 0.5;
E1 (8 0 0 7) 7413;
E2 (19 0 0 11) 7413;
E3 (12 0 0 9) 7413;
E4 (10 0 0 13) 7413;
V1 (1 0);
END;

ANALYZE SSS;
INFREQ 0.001 20000 LIN 50;
SET V1 AC 1 0;
PRINT VDB(8) VDB(19) VDB(12) VDB(10);
PLOT VDB(8) VDB(19) VDB(12) VDB(10);
END;

END;
```



- •Dynamic scaling.
- •Minimum Capacitor Spread Scaling.

The Dynamic Range (DR) Scaling of Capacitors

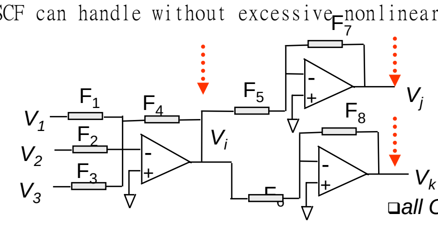
2010/5/3

Ron-Yi Liu

The Optimization of the dynamic range using Scaling Procedures :

⇒ Improve the actual performance and avoid the saturation of each *OP AMP*.

- Let all branches connected to the *output* terminal *OAi* be modified such that their Q/Vi (transfer functions) in F4, F5 and F6 are multiplied by a positive factor *K*.
- This can be achieved by multiplying all capacitors in these branches by *Ki.*
- Since the input branches and their voltages were unchanged, the charge flowing in the feedback branch is remain at its original value. $\Delta Q_4(4) = -\Delta Q_1(4) - \Delta Q_2(4) - \Delta Q_3(4))$
- The voltage scaling does not affect charge flowing from the scaled branch to the rest of the circuits. ⇒ Only Vi -> Vi/Ki, all other voltages or charges are not affected.
- Vmax/Ap > Vin,max , Ap : *passband gain*, Vin,max is the max. input signal which the SCF can handle without excessive nonlinear distortion.



$$V_i^*(Z) = \Delta Q_4(Z)/[KiF_4(Z)] = V_i\ (Z)/Ki$$

$$\Delta Q_5^* = F_5^*(Z)V_i^*(Z) = KiF_5(Z)V_i\ (Z)/Ki$$

$$= F_5(Z)V_i\ (Z) = \Delta Q_5$$

❑*all Op-Amp outputs should be scaled to 0dB.*

The Optimum Dynamic Scaling of Capacitors in SCFs

- *For maximum dynamic range, all Op-Amp outputs should be scaled to 0dB such that (at its own maximum frequency) each saturates for the same input voltage level.*

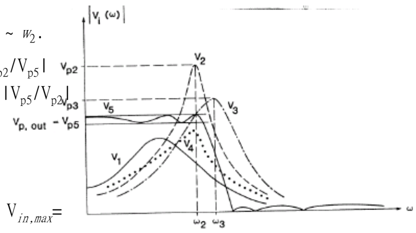
1. OA_2 will *saturate* before OA_5, because $|V_2| > |V_5|$ for $w \sim w_2$.
2. $V_{in,max} = V_{max}/A_2$, $A_2 = |V_{p2}/V_{in}|$, $Ap = |V_{p5}/V_{in}|$ $\Rightarrow$ $A_2 = Ap\,|V_{p2}/V_{p5}|$
3. $V_{in,max} = V_{max}/A_2 = [V_{max}/Ap]\,|V_{p5}/V_{p2}| < V_{max}/Ap$. since $|V_{p5}/V_{p2}| < 1$.

$\Rightarrow$ Maximum Vin decrease, then Dynamic range decrease.

- Reduce V_2 by scaling, $V'_2(w) = V_2(w)/K_2$, $K_2 = V_{p2}/V_{p5}$.

$\Rightarrow$ V'_2 has a peak value V'_{p2} (which is equal to V_{p5}), then $V_{in,max} = V_{max}/Ap$.

- Similarly, $K_3 = V_{p3}/V_{p5} < 1$, $K_1 = V_{p1}/V_{p5} < 1$, $K_4 = V_{p4}/V_{p5} < 1$.
- Scaling for optimum dynamic range may also reduce the *sensitivity* to the finite Op-Amp gain effects



The Minimum Capacitor Scaling of SCFs

- *The Optimization of the Min. Capacitor Scaling Procedures* :

  => Reduce the overall silicon area (The total capacitor value in SCFs).

- Let all branches connected to the *input* terminal *OAi* be multiplied by a positive factor m_i.

=> C_i --> $m_i\, C_i$, Q_n (n=1, 2, 3 and 4) --> $\Delta Q'_n = m_i \Delta Q_n$

$$V_i^* = \frac{\Delta Q_4'}{F_4'} = \frac{m_i \Delta Q_4}{m_i F_4} = \frac{\Delta Q_4}{F_4} = V_i$$

=>The input charges Q_5 and Q_6 also remain the same.

- The scaling by m_i make all output voltages unchanged. (Only the charges in the scaled branches multiplied by m_i.)

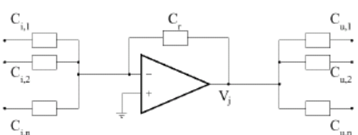
  =>Effective in reducing the *capacitor spread* and the total capacitance in SCFs.

- $C_{i,min}$ among all capacitors contained in these four branches is located.

  => All capacitors contained in these four branches are multiplied by $m_i = C_{min}/C_{i,min}$.

- The smallest capacitance become C_{min}

and all Op-Amp voltages remain unaffected.



- **After voltage scaling, all capacitors are scaled to minimum values in order to save area**

If $\dfrac{C_{min}}{\min\{C_{i,1},\ldots,C_{i,n},C_r\}} \equiv m_j$, then $C_{i,1}, C_{i,2}, \ldots, C_{i,n}, C_r$ are given the new values $m_jC_{i,1}, m_jC_{i,2}, \ldots, m_jC_{i,n}, m_jC_r$

Capacitor Layout in SC circuits

Reference: Martin's book, pp.108~112.

❑Since the thickness of S_iO_2 is 700~5,000 A, typical MOS capacitor C = 0.25~0.5 fF/um^2. Typical ***capacitor spread*** is Cmin/Cmax = 20~40 for SC circuits.

- •Square type unit capacitor C_u in SCF⇒ for the same area-perimeter ratio.
- •common-centroid layout.⇒ *Low sensitivity to the oxide thickness gradient.*

❑Non-unit-sized capacitor : 1 ~ 2 C_u .

❑The overall capacitors connected to Op Amp's output is the loading capacitor CL of Op Amp spec. ⇒ remember to define the CL in Op carefully before Op Amp design.

DR scaling Min Cap scaling

Table 1 : Capacitor values

Switched-capacitors

C_{in}	1		2
C_1	1	0.8785	1.75
C_2	1	2.1815	4.37
C_3	1	0.8785	6.89
C_4	1	3.2916	5.96
C_5	1	1	1
C_6	1	1	2
C_7	1	0.8785	1.59
C_8	1	0.5515	1
C_9	1	1	3.19
C_{10}	1	.05515	6
C_{11}	1	2.7510	8.77
C_{12}	1	0.5515	1
C_{13}	1	0.4274	1.36
C_{14}	1	0.8929	1.79
C_{15}	1	0.4274	1
C_{16}	1.1650	0.4979	1
C_{17}	0.2311	0.1275	1
C_{18}	0.1046	0.0919	1

Integrating capacitors

C_{I1}	2.3764	2.0877	4.18
C_{I2}	0.7773	1.6957	13.3
C_{I3}	0.4850	1.5964	1.59
C_{I4}	3.9820	3.9820	7.22
C_{I5}	5.1474	2.8387	9.05
C_{I6}	0.3519	0.9680	10.53
C_{I7}	0.8313	0.7422	1.73
C_{I8}	2.2910	0.9791	1.96

Transmission zeros

C_A	0.5684	0.3135	1
C_B	0.5684	-0.4993	1

Cmax/Cmin=81

Cmax/Cmin=13

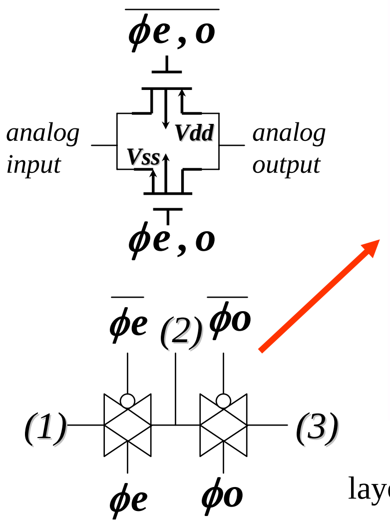
SWITCAP II Simulator

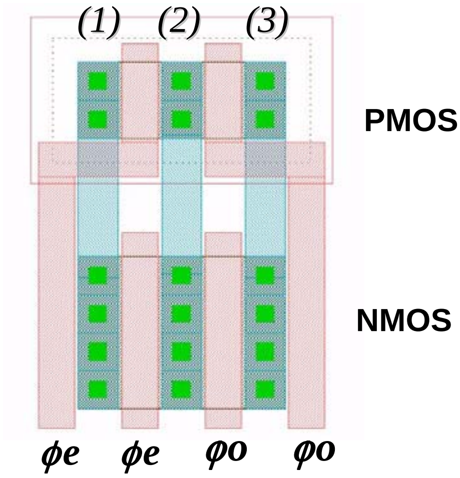
- Faster and very accurate Simulated by SWITCAP II for Filter specification checking include:
  - The frequency-domain and time-domain analysis in addition to Sampler and Hold effects.
  - The finite Gain and Bandwidth effects in Op Amp, and finite Ron resistance in SWITCH.
  - The dynamical capacitor scaling in each op amp output, and minimum capacitor scaling in each virtual GND.
  - Noise and Capacitor sensitivity Analysis.
  - SC Filter simulation is according to the capacitor's ratio and sampling frequency Fs in frequency domain and time domain. ⇐ unit capacitor is relative (not absolute) numerical, such as : Cu=1.0 (5 um X 5 um ~10 um X 10 um).

Double-Pole-Double-Throw Switch

1998/6/19

Ron-Yi Liu



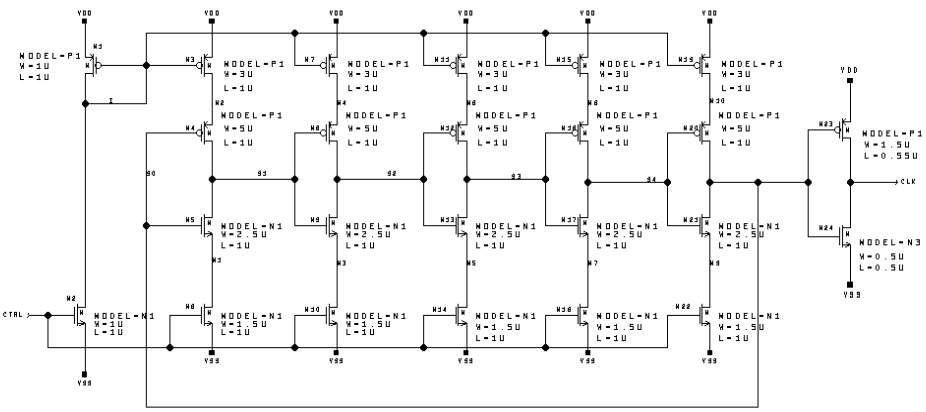


layout area : 8.3μm x 11.25μm

VCO Circuit Structure

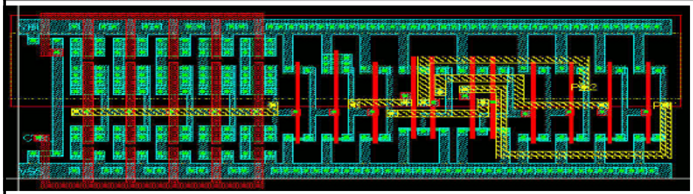
2010/5/3

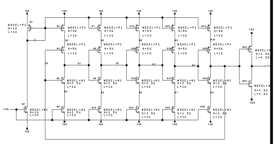
Ron-Yi Liu

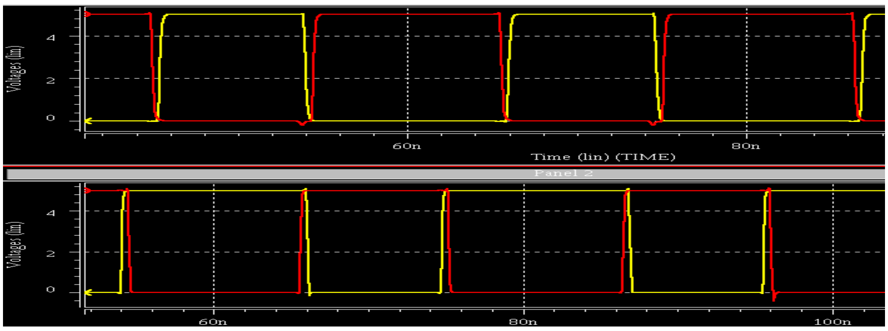


VCO Circuits Layout and HSPICE Simulation Results

2010/5/3





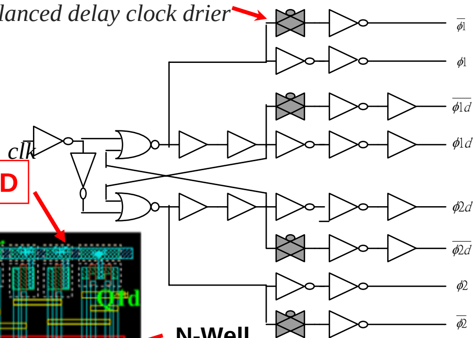


The Four-Phase Non-overlap Clock Generator

1998/6/19

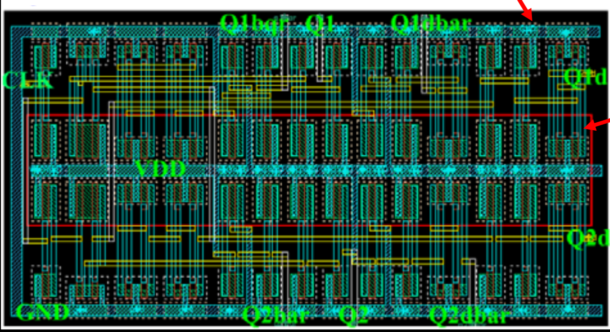
- Duty cycle=40~45%, to avoid ***clock overlapping***.
- Delay circuits is by even number of inverters.

Balanced delay clock drier



$W \times L = 107.95*53.5=5775.325 \ um^2$

GND



N-Well

VDD

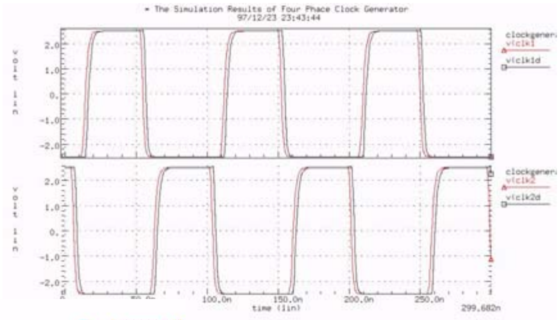
GND

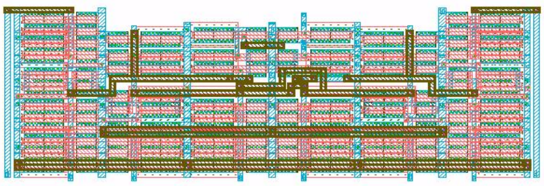
The Simulation Results of Four-phase Non-overlap Clock Generator

Ron-Yi Liu

Post-simulation

CMOS 0.5um 2P2M process





layout area : 138 μm x 48 μm

- duty cycle = 41.2 %
- delay = 2.5 ns
- power = 1.595nW

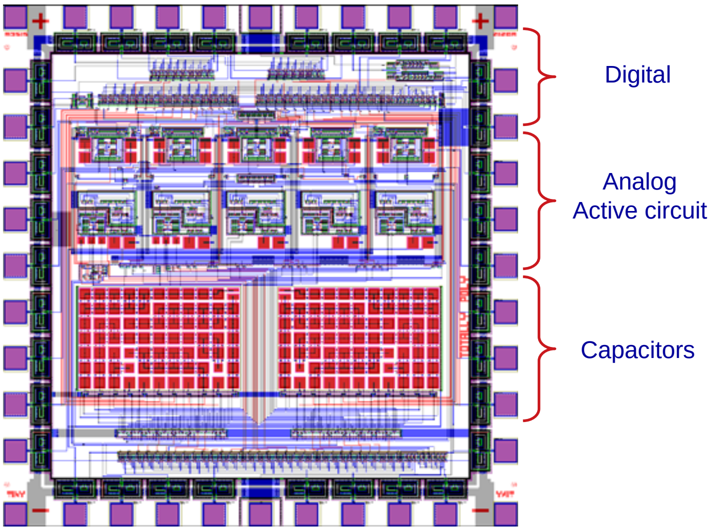
Design and Layout of SC Circuits

Ron-Yi Liu

- **Check LP, BP and HP Filter band edge, Sampling frequency about: signal magnitude's S/H effect and frequency-axis prewarping.**
- **Design by Cascade approach (directly in Z-domain) or Ladder approach (analog s-domain)?**
- **Check the Filter spec. (order, pass- and stop-band ripple, phase, transition band, ..) about filter type of Butterworth, Chebyshev, Elliptic,..from CAD (MATLAB, Filter solution,..) for H(z) [biquadratic structure] or H(s) [RLC-ladder structure].**
- **Realize the SC (Fully Differential) circuits from digital H(z) or analog H(s).**
- **Simulate the SC circuits by SWITCAP II and check the dynamic scaling for these capacitors around each Op amp's output and minimum capacitor scaling for these capacitors around each Op amp's input.**
- **Check the Capacitor's spread and unit capacitor.**
- **Check Op Amp design to meet the required Gain and Bandwidth.**
- **Overall SC circuits Layout and post-simulation.**

SC Circuit Layout

(Single Ended-Op Amp)

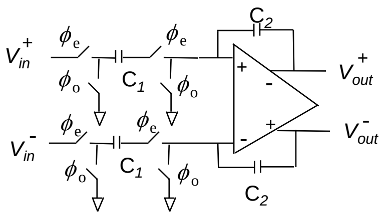


The Differential-Type SC Integrators

- *This a standard and important strategy, especially in low-voltage processes.*
- *A new degree of freedom* :

=> The single-ended circuits: A positive gain with output delayed $Z^{1/2}$ (numerator).

=> The differential circuits: The sign of gain may be chosen arbitrarily by interchanging *input* or *output* terminals



$$V_{out}^{+} = -V_{out}^{-} = A_v(V_{in}^{+} - V_{in}^{-})$$

$$H_1(z) = (V_{out}^{+} - V_{out}^{-}) / (V_{in}^{+} - V_{in}^{-})$$

$$= -\frac{C_1}{C_2}\frac{Z^{1/2}}{(Z^{1/2} - Z^{-1/2})} \quad \textit{Phase-2 output}$$

$$H_2(z) = -\frac{C_1}{C_2}\frac{Z^{-1/2}}{(Z^{1/2} - Z^{-1/2})} \quad \textit{Phase-1 output}$$

Distortion Cancellation in Differential-SC Integrators

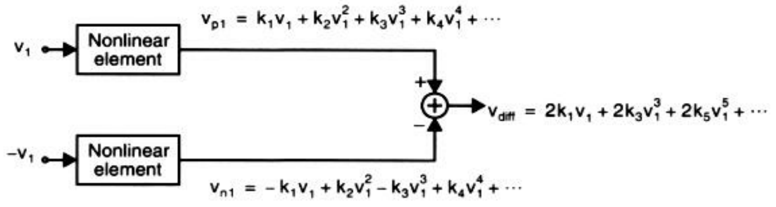
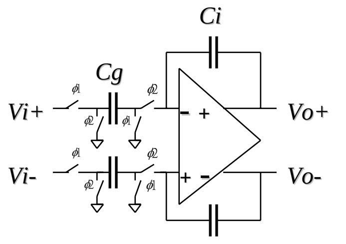


Fig. 10.17 Demonstrating that even-order distortion terms cancel in fully differential circuits if the distortion is symmetrical around the common-mode voltage. Here, the common-mode voltage is assumed to be zero.

- *The signals are the difference between two voltages in symmetrical circuits of common-mode type.*
- *Noise as a common-mode signal and does not affect the signal.*
- *Only very small odd-order distortion terms. ⇒ Better CMRR and PSRR.*
- *Better noise rejection (Against offset and charge injection).*
- *Better frequency response and Slew Rate (SR).*

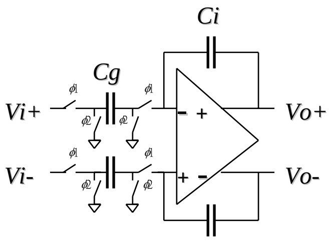
The Basic Fully-Differential Switched-Capacitor Integrator

- *Noninverting integrator*



$$H(z) \equiv \frac{Vo(z)}{Vi(z)} = \left(\frac{Cg}{Ci}\right)\frac{z^{-1}}{1-z^{-1}}$$

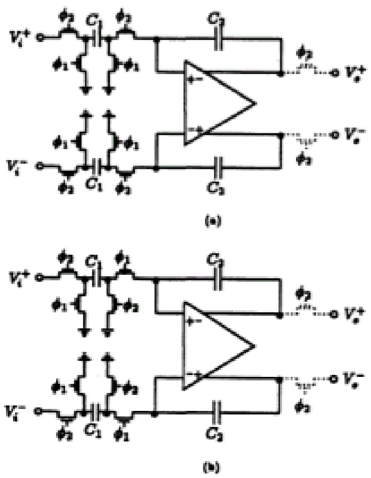
- *Inverting integrator*



$$H(z) \equiv \frac{Vo(z)}{Vi(z)} = -\left(\frac{Cg}{Ci}\right)\frac{1}{1-z^{-1}}$$

- *Symmetrically Balanced and More components (switches, capacitors and OP Amps).*
- *Thermal noise increases due to the added components and switching operations.*
- *Need common-mode feedback or common-mode bias circuits.*

LDI Fully-Differential Switched-Capacitor Integrator



•It is a very simple integrator.

Inverting Integrator

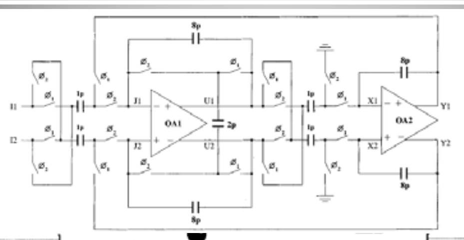
$$H(z) \equiv \frac{Vo(z)}{Vi(z)} = -\left(\frac{Cg}{Ci}\right)\frac{1}{1-z^{-1}}$$

Non-Inverting Integrator

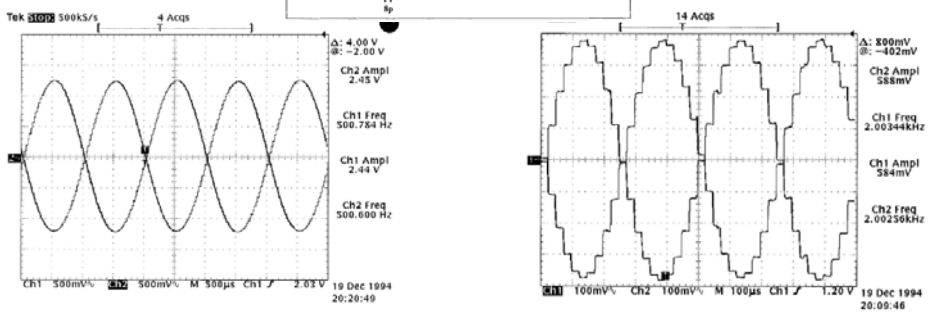
$$H(z) \equiv \frac{Vo(z)}{Vi(z)} = \left(\frac{Cg}{Ci}\right)\frac{z^{-1}}{1-z^{-1}}$$

•It is very important in the design of (fully differential) Sigma-Delta ADC design .

Biquadratic fully differential SCF Filter



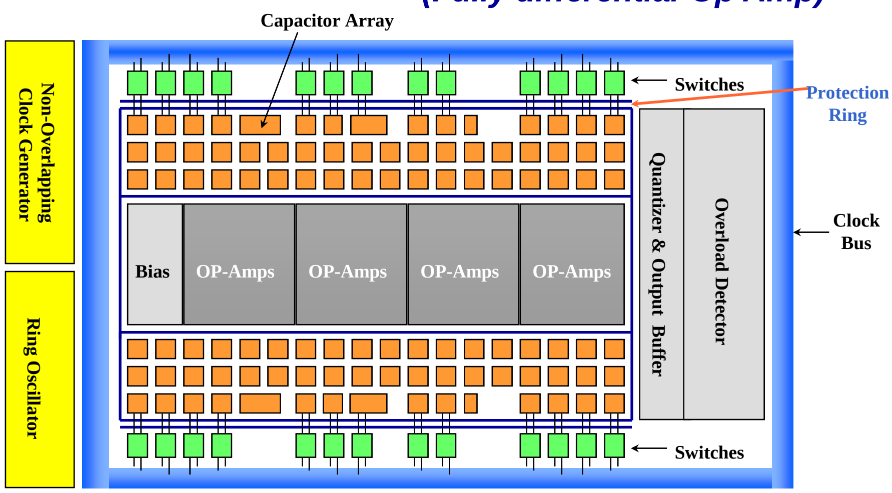
■1-V differential input at two circuit frequencies.
■Clock frequency is 40 kHz.



Filter output for 1-V differential input: (a) 500 Hz and (b) 2 kHz.

The Floor Placement of Four-order Sigma-Delta SC Modulator

(Fully differential-Op Amp)



Switched Capacitor Circuits Design

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